TB9100 base station

Reciter Service Manual

MBA-00017-01
Issue 1
January 2006

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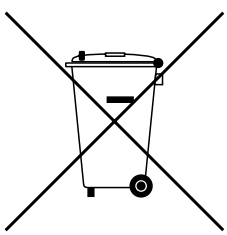

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Contents

Preface

Scope of Manual

Welcome to the TB9100 Reciter Service Manual. This manual provides servicing information for the TB9100 reciter. All other TB9100 base station servicing information is the same as the information provided in the TB8100 Service Manual.

Enquiries and Comments

If you have any enquiries regarding this manual, or any comments, suggestions and notifications of errors, please contact Technical Support (refer to "Tait Contact Information" on page 2).

Updates of Manual and Equipment

In the interests of improving the performance, reliability or servicing of the equipment, Tait Electronics Limited reserves the right to update the equipment or this manual or both without prior notice.

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Terminology

To align with the PowerPC documentation, this document uses the term "word" to refer to a 32-bit number; a 16-bit number is referred to as a "half-word". This convention is continued through the sections in this document relating to the DSP. However, other documentation on the DSP may refer to a "word" as being a 16-bit quantity.

In this text, the term "asserted" refers to a signal being driven to its active state, regardless of whether that active state is logic high or logic low. Conversely, the term "negated" refers to a signal being driven to its inactive state.

Signal Naming Convention

Active low logic signals are indicated in the text with an overbar or by a negation bubble on schematic symbols. However, due to limitations of the schematic editor, active-low signal names have been indicated on the schematics with an "_N" suffix.

Hexadecimal numbers are indicated with a "0x" prefix. Binary numbers are indicated with a "0b" prefix.

Bus Numbering Convention

Signals that are grouped in a bus will be labelled thus:

Bus_name[most_significant_bit .. least_significant_bit]eg. D[31..0]

Note The PowerPC architecture defines the numbering of data and address buses in the reverse order to normal convention. Hence, D0 is the msb and D31 is the lsb of the data bus. Other devices in the ASIF use conventional numbering order; the transition from PowerPC numbering order to normal numbering order occurs at the external pins of the PowerPC processor.

Associated Documentation

TB8100 Service Manual.

TB9100 Specifications Manual.

TB9100 Installation and Operation Manual.

TB9100 Customer Service Software User's Manuals and online Help.

TB9100 Calibration Kit User's Manual and online Help.

TB9100 Network Installation Guide.

Technical notes are published from time to time to describe applications for Tait products, to provide technical details not included in manuals, and to offer solutions for any problems that arise.

All available TB9100 product documentation is provided on the CD supplied with the base station[1]. Updates may also be published on the Tait Technical Support website (http://support.taitworld.com).

Publication Record

Issue	Publication Date	Description
1	January 2006	First release

Glossary

1PPS	One Pulse Per Second
100BaseT	100Mbps ethernet over a twisted pair network
10BaseT	10Mbps ethernet over a twisted pair network
2W	Two wire, an audio interface with a single cable pair shared for both transmit and receive signals
4W	Four wire, an audio interface with separate cable pairs for transmit and receive signals
APCO	Association of Public Safety Communications Officers, a US body of public safety communications users (eg. Police, Fire) which defines standards on behalf of its members
ASIF	APCO SIF, the system interface from a base station to an APCO network. Also known as the network board.
ATM	Asynchronous Transfer Mode
BD	Buffer Descriptor
BDM	Background Debug Mode, a method of debugging software on a RISC processor
BGA	Ball Grid Array, a type of integrated circuit package
Big Endian	A memory ordering scheme where the most-significant byte of a word occupies a lower memory address than the least-significant byte c.f. Little Endian

1. Technical notes are only available in PDF format from the Tait support website. Consult your nearest Tait Dealer or Customer Service Organization for more information.

BRG	Baud Rate Generator
BS	Refers specifically to the Reciter control element of the base station
CPM	Communications Processor Module, a RISC processor dedicated to handling communications interfaces
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CTS	Clear to Send
DARAM	Dual-Access RAM
DCE	Data Communications Equipment
DMA	Direct Memory Access, a method of moving data to/from memory with hardware assistance
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor, a processor specialized for numerical processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLB	Data Translation Lookaside Buffer
DTR	Data Terminal Ready
E&M	Ear and Mouth, a simple DC signalling scheme used in telecom networks
E2PROM	Electrically Erasable Programmable Read Only Memory
EDO	Extended Data Out, a type of DRAM
EHPI	Enhanced Host Port Interface, now renamed as HPI
EMC	Electromagnetic Compatibility
EMIF	External Memory Interface
EPROM	Erasable Programmable Read Only Memory
ESD	Electrostatic Discharge
FEC	Fast Ethernet Controller
FIFO	First-In/First-Out, a variable length shift register that supports queuing of data streams
FLASH	A type of electrically erasable programmable read-only memory. Usually not byte-erasable.
HPI	Host Port Interface, an interface between a DSP and its host processor
GPCM	General-purpose Chip-select Machine, a basic user programmable memory controller
GPR	General purpose register

Harvard architecture	A type of computer architecture that utilizes separate memory spaces for executable code and data. cf. von Neumann architecture
HW	Hardware
I^2C	Inter-Integrated Circuit, a serial communications interface mainly intended for interconnecting ICs contained within a single PCB
IPN	Internal Part Number, TEL's internal part numbering system.
ITLB	Instruction Translation Lookaside Buffer
IU	Integer Unit
JTAG	Joint Test Action Group, a test interface specification for PCB assembly testing
Little Endian	A memory ordering scheme where the least-significant byte of a word occupies a higher memory address than the most-significant byte c.f. Big Endian
LRU	Least Recently Used, a method of updating cache memory contents
lsb	Least significant bit
LSU	Load/Store Unit
LVTTL	Low Voltage TTL, logic specified for operation at 3.3V supply and compatible with 5V TTL family logic levels ie. VIH = 2.0V and VIL=0.8V
MAC	Media access controller, an ethernet controller
McBSP	Multi-channel Buffered Serial Port
MII	Media Independent Interface, an interface for ethernet PHY devices
MIPs	Million Instructions Per Second
MMU	Memory Management Unit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPC	MPC859TPZ133 PowerQUICC microprocessor
NMI	Non-maskable interrupt
OTP	One Time Programmable, a non-volatile memory device that cannot be erased and reprogrammed after initial programming
msb	Most significant bit
PBGA	Plastic BGA
PCM	Pulse Code Modulation

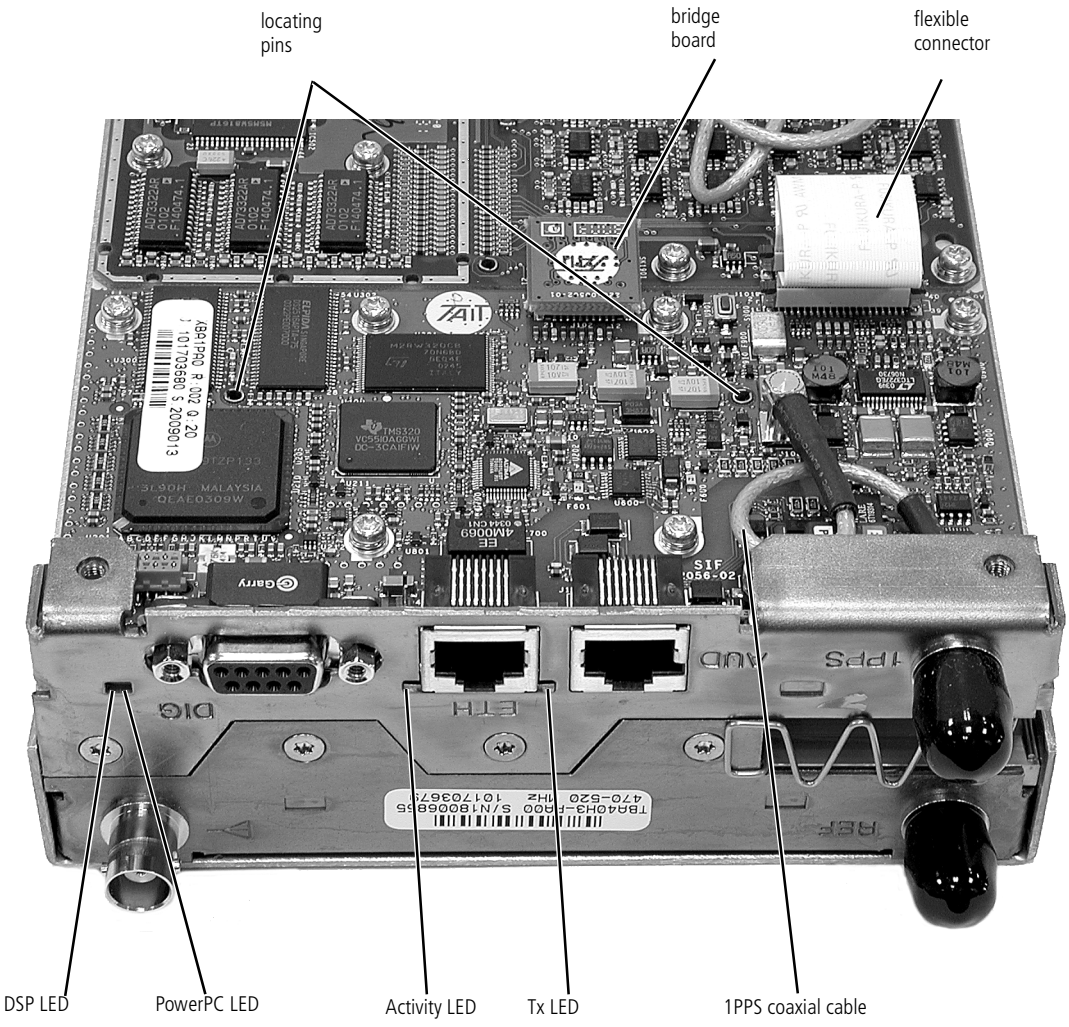
PCMCIA	Personal Computer Memory Card International Association
PCM highway	A TDM bus typically used for interconnecting CODECs and DSPs
PHY	Ethernet PHYsical interface
PIT	Periodic Interrupt Timer
PLL	Phase-Locked Loop
PowerPC™	A microprocessor architecture defined by IBM and Motorola
PowerQUICC™	PowerPC Quad Integrated Communications Controller, a PowerPC integrated with a QUICC
pp	Peak to Peak
PPC	PowerPC™
ppm	Parts Per Million
PSTN	Public Switched Telephone Network
QUICC™	Quad Integrated Communications Controller, a version of a CPM
Reciter	Receiver/Exciter - the RF signal handling parts of the base station excluding the power amplifier
RISC	Reduced Instruction Set Computer, a general-purpose processor
RS-232	A standard defining electrical parameters for serial interfaces
RSSI	Received Signal Strength Indication
RTS	Request To Send
Rx	Receive
RxD	Receive Data
SARAM	Single-Access RAM
SCC	Serial Communications Controller
SDMA	Serial DMA
SDRAM	Synchronous Dynamic Random Access Memory
SIF	System Interface
SIO	Synchronous Input/Output, a simplified version of SPI
SIU	System Interface Unit
SMC	Serial Management Controller
SMI	Serial Management Interface, an interface for management and control of ethernet PHYs

Software	When 'software' is not otherwise qualified, it refers to the ASIF software that is the subject of this document
SPI	Serial Peripheral Interface, a simple serial communications interface mainly used for I/O expansion on microprocessors
SPR	Special Purpose Register, a type of register used for configuration and control of the PowerPC CPU core
SRAM	Static Random Access Memory
SW	Software
TAP	Test Access Port
TDM	Time Division Multiplex
Telco	Telephone Company
TSA	Time Slot Assigner
TTL	Transistor-Transistor Logic, an early bipolar logic family
Tx	Transmit
TxD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
UPM	Universal Programmable Machine, a type of user programmable memory controller
USART	Universal Synchronous/Asynchronous Receiver/Transmitter
UTOPIA	Universal Test & Operations PHY Interface for ATM
VCTCXO	Voltage-Controlled Temperature Compensated crystal Oscillator
Vocoder	Voice coder, a program that encodes voice signals into a digital representation, or vice versa
von Neumann architecture	A type of computer architecture that combines executable code and data into the same memory space. cf. Harvard architecture.

1 Replacing the Network Board

This section describes how to troubleshoot and replace a faulty reciter network board. Servicing procedures for the reciter digital board and the reciter RF board are covered in the TB8100 Service Manual.

Figure 1.1 Network Board



1.1 Equipment Required

- Anti-static work environment
- PC with Ethernet cable.
- Torque screwdriver (4.5in-lbs) with Torx T-10 bit
- TB9100 subrack (PA not required)

- Power cable, PMU to reciter
- Ethernet switch or hub (if available)

1.2 Troubleshooting

Before replacing the network board, carry out the following tests on the reciter to exclude other causes and to verify that the fault actually lies in the network board hardware.

1. Connect the reciter to the subrack via the I^2C bus and the DC power cable. Apply power. This checks whether the digital board is working and receiving communications from the network board.
   a. If no LEDs light on the control panel or rear panel, check that power is being supplied to the reciter.
   b. If the control panel power LED comes on first, followed by the others, the digital board firmware is working.
   c. If the control panel LEDs all remain on for more than 30 seconds, the digital board is not receiving communications from the network board.

2. Carry out a visual check of the LEDs on the rear of the reciter to check the network board's functional subsystems.
   a. If all LEDs are off, open the reciter and check the flexible connector (it supplies power to the network board). Replace if faulty (see step 5. on page 17).
   b. If the PowerPC LED is flashing quickly (2 Hz), the operating system kernel is running. If it is flashing slowly (0.5 Hz), only the bootloader is running. If the Power PC LED does not flash, check that there is power to the board. The Tx LED should flash once when power is connected. If it does, power is present, so the bootloader must be faulty (see step 7. on page 15).
   c. If the orange LED is flashing, the DSP software in the network board is executing code. If the LED doesn't flash, open the reciter and check that the bridge board is connecting properly.
   d. The green Ethernet LED should flash if the digital line is connected to an Ethernet switch. This indicates that the digital line is receiving activity pulse from the Ethernet switch.

3. Connect to the network board's serial port to test its functioning.
   a. Connect your PC to the 9-pin serial connector on the back of the reciter.
   b. Run a program such as HyperTerminal, Teraterm or minicom.
   c. Select the following port settings: 57600 baud, 8 bits, no parity, 1 stop bit, no flow control.
   d. Press the 'Enter' key. If a login prompt appears, the kernel is running. If the bootloader prompt (=>) appears, contact Tait for

assistance with re-loading the kernel and application software.

e. Note down the reciter's IP address that is displayed at the login prompt and close the session.

4. Connect the PC to the network board over its digital Ethernet line.

   a. Using the IP address you noted down, ping the reciter from the Windows command prompt. If there is a response, the network board's Ethernet interface circuitry is functioning in both directions. If there is no response, replace the board.

   b. Attempt to connect the CSS to the reciter. If this is successful, the network board application is running. Check the Alarm Status screen for reciter alarms. Carry out the control panel LED diagnostic test.

5. If there is no obvious hardware fault, replace the current firmware and/or kernel to see if this fixes the problem.

   a. If possible, use the CSS to upload the firmware.

   b. Otherwise, follow TN-997 to replace the kernel and/or the firmware using telnet and a TFTP server.

6. Exclude the base station configuration as the source of problems by programming in a new configuration.

   a. In the CSS, connect to the reciter.

   b. Read the configuration and save it to file.

   c. Select File > New.

   d. Modify the new configuration as necessary.

   e. Program the new configuration into the reciter, leaving its current IP address and netmask.

7. Attempt to access the bootloader prompt. If this is unsuccessful, the bootloader is faulty. The reciter will need to be returned to Tait Electronics Limited for the bootloader to be repaired.

8. If the network board fails some or all of the above tests, replace it as described below.

1.3 Before You Start

Make sure you have a backup of the current base station configuration. Obtain it from the customer or, if possible, use the CSS to connect to the reciter, read the configuration, and save it to a file.

1.4 Removing the Faulty Board

1. Remove the M3 Torx screws securing the cover on the digital side of the reciter. Lift off the cover. (The digital side is nearest to the 9-way D and RJ45 connectors.)
2. Remove the two M3 Torx screws that secure the rear panel on the digital side of the reciter.
3. Disconnect the coaxial cable from the network board and lift off the bridge board.
4. Disconnect the flexible connector by gently levering up the lugs on the ends of the latch. The flexible connector springs free.
5. Remove the eight M3 Torx screws that secure the network board to the heatsink.
6. Carefully lift the network board off the locating pins and remove it from the heatsink.

Important Flexing the board may damage the PCB tracking or break solder joints.

If the board is a snug fit on the locating pins, you may have to very gently lever the board with a screwdriver, beginning at the right-hand side (as viewed in Figure 1.1), to get it to lift.

1.5 Replacing the Board

Important Be very careful to keep the replacement board scrupulously clean. The board is densely populated and the smallest particle of conductive dust can cause a short.

Important Make sure the insulator sheet is correctly positioned and flat on the heatsink. Although this sheet is an electrical insulator, it is also thermally conductive and must allow the PCB to sit as flat as possible to provide effective heatsinking. **Operating the reciter without the insulator sheet in place will result in permanent damage to the digital or system interface PCBs.**

1. Make sure that there is no debris on the underside of the network board.
2. Position the replacement network board over the locating pins and press it down over them so that it is firmly seated against the insulator sheet on the heatsink.

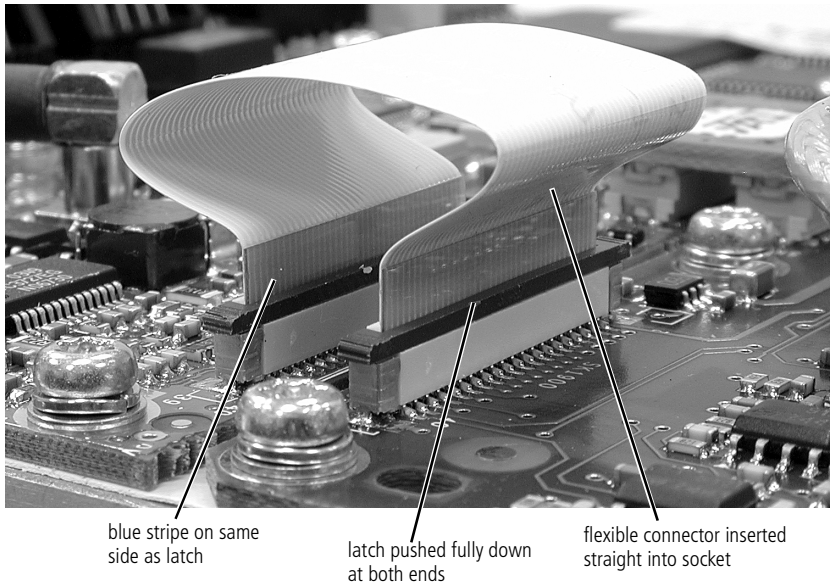
3. Replace the eight M3 Torx screws and tighten them to the correct torque.

Important Do not exceed 4.5in-lbs of torque; greater torque settings may damage the PCB. Inadequately tight screws can affect the EMC properties of the board.

4. Position the bridge board above the sockets and the right way round. Press it into place.

5. Carefully reconnect the flexible connector as shown in Figure 1.2. (If required, fit a new flexible cable. It must be correctly formed to prevent excessive stress on the cable or the connector.) Make sure that the cable is properly located before pressing the latch down.

Figure 1.2 Reconnecting the Flexible Connector



6. Reconnect the 1 PPS coaxial cable.

7. Replace the rear panel and the reciter cover. Tighten the Torx screws to the correct torque. Inadequately tight screws can affect the EMC properties of the board.

8. Return the faulty board to Tait.

1.6 Restoring the Configuration

1. Connect the CSS to the reciter using the correct IP address (network boards are given the IP address 192.168.1.2 in the factory.)
2. Restore the base station's configuration, overwriting the IP address.
3. Reset the reciter. On power-up, the reciter uses the new IP address.
4. Use the procedures in the Troubleshooting section above to verify correct operation of the network board.

2 Reciter Circuit Descriptions

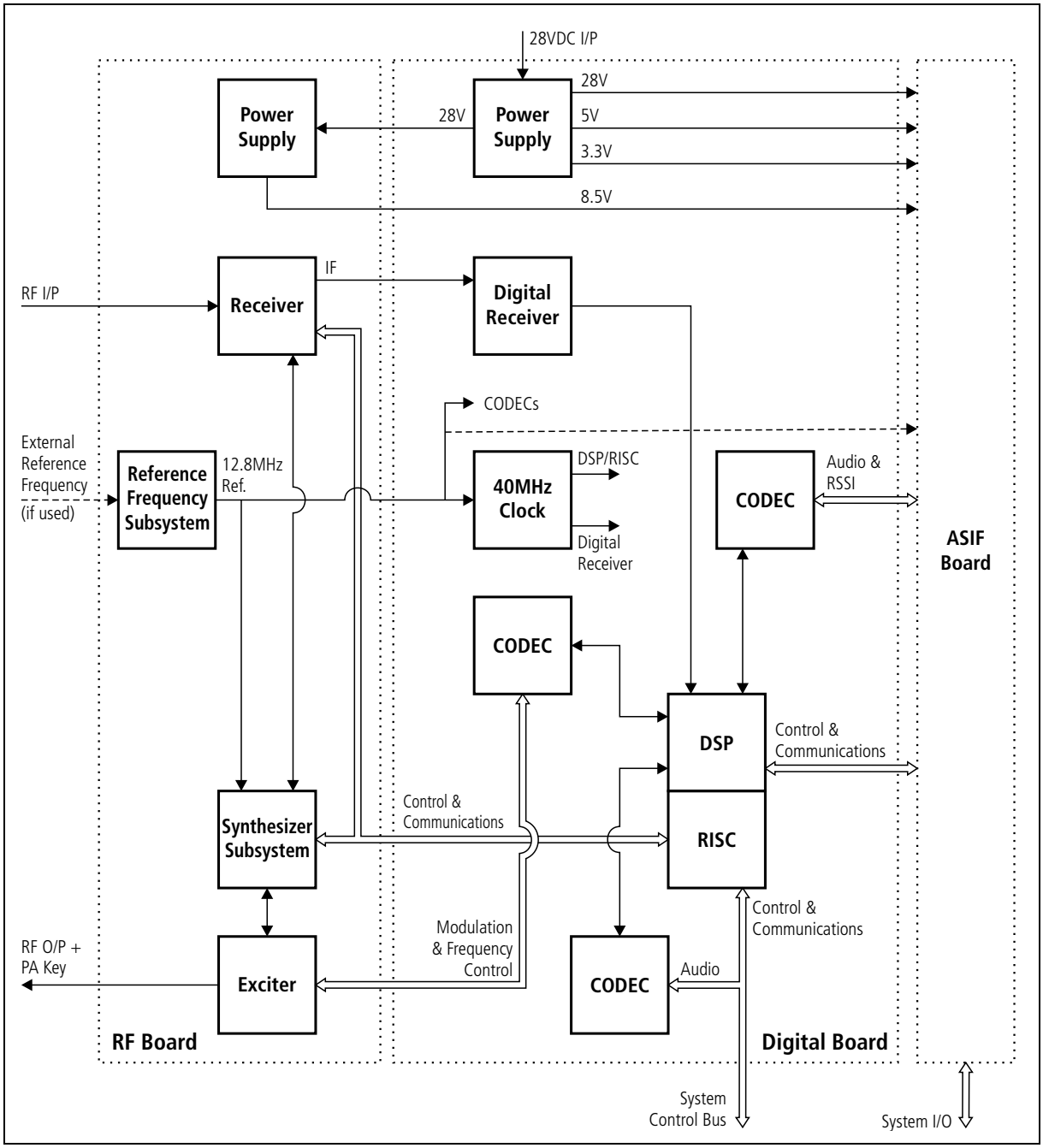
This chapter describes the circuitry used in VHF and UHF reciters. Much of this circuitry is common to both frequency bands, and is therefore covered by a single description in this chapter. Where the circuitry differs between VHF and UHF, separate descriptions are provided for each frequency band. In some cases the descriptions refer to specific VHF or UHF bands or sub-bands, and these are identified with the letters listed in the following table.

Table 2.1 TB9100 frequency bands

	Frequency Identification	Frequency Band and Sub-band
VHF	B band	B1 = 136MHz to 174MHz B2 = 136MHz to 156MHz B3 = 148MHz to 174MHz
UHF	H band	H0 = 400MHz to 520MHz H1 = 400MHz to 440MHz H2 = 440MHz to 480MHz H3 = 470MHz to 520MHz

The reciter comprises three PCBs: an RF, a digital, and a network PCB. These PCBs are mounted on a central chassis/heatsink. Figure 2.1 on page 20 shows the configuration of the main circuit blocks, and the main inputs and outputs for power, RF and control signals. The locations of the main circuit blocks on the PCBs are shown in Figure 5.1 on page 36.

Figure 2.1 Reciter High Level Block Diagram



3 Digital Circuitry

Refer to Figure 3.1 on page 24.

3.1 Digital IF

3.1.1 VHF Reciter

The heart of the digital IF system is the 14-bit analog-to-digital converter (ADC). This is a high-speed device, with a multi-staged "pipeline" architecture, which is clocked and outputs samples at 40MSPS (megasamples per second). The analog IF input of the ADC is a differential structure, and the output is via a 14-bit parallel bus.

The band-limited 16.9MHz IF signal is sampled by the ADC at 40MSPS. The sampling process results in images of the input signal appearing at other frequencies so that the ADC behaves in a similar fashion to a mixer. The digital output therefore contains the wanted signal and the images, which can be digitally processed to extract one of the many signals. The desired IF is at 16.9MHz.

The digital downconverter (DDC) digitally downconverts the 16.9MHz IF to baseband. This is achieved by digital mixing with a numerically controlled oscillator (NCO). The mixing process is done using in-phase and quadrature methods to achieve image rejection, and allows channel filtering to be applied before the signal is passed to the digital signal processor (DSP) for demodulation. The digital channel filtering also decimates the sample rate down to 50kSPS (kilosamples per second) for the DSP.

3.1.2 UHF Reciter

The heart of the digital IF system is the 14-bit analog-to-digital converter (ADC). This is a high-speed device, with a multi-staged "pipeline" architecture, which is clocked and outputs samples at 40MSPS (megasamples per second). The analog IF input of the ADC is a differential structure, and the output is via a 14-bit parallel bus.

The band-limited 70.1MHz IF signal is sub-sampled by the ADC at 40MSPS. The sub-sampling results in images of the input signal appearing at other frequencies so that the ADC behaves in a similar fashion to a mixer. The digital output therefore contains information in the form of images, which can be digitally processed to extract one of the many signals. The lowest frequency image for the 70.1MHz IF and 40MHz clock is at 9.9MHz.

The digital downconverter (DDC) digitally downconverts the desired image (9.9MHz) to baseband. This is achieved by digital mixing with a numerically controlled oscillator (NCO). The mixing process is done using in-phase and quadrature methods to achieve image rejection, and allows channel filtering to be applied before the signal is passed to the digital signal processor (DSP) for demodulation. The digital channel filtering also decimates the sample rate down to 50kSPS (kilosamples per second) for the DSP.

3.2 Digital Signal Processor (DSP)

The DSP is responsible for software processing of digitized signals in the receiver and transmitter. The processing word width is 16-bit fixed point. There are 96 kilobytes of on-chip program memory, and 64 kilobytes of on-chip data memory. Although no external memory is used, the external memory interface is connected to the DDC for initialization and configuration.

3.2.1 Transmit Functions

The DSP performs the following transmit functions:

- CTCSS and DCS sub-audible signal generation
- CWID generation
- pip tone generation
- audio filtering: including removal of sub-audible components, pre-emphasis and low pass filtering
- signal path switching
- signal level adjustment
- peak FM deviation limiting
- FM signal generation by controlling the dual point modulator
- calibration parameter estimation
- line level monitoring.

3.2.2 Receive Functions

The DSP performs the following receive functions:

- detection of CTCSS and DCS signalling
- audio filtering: including removal of sub-audible components, de-emphasis and low pass filtering
- signal path switching
- signal level adjustment
- FM demodulation of the base band signal

- RSSI measurement for monitoring and RSSI signal voltage output
- SINAD measurement
- measurement and detection for control of the audio mute
- calibration parameter estimation
- line level monitoring.

3.2.3 Serial Ports

The DSP has three synchronous serial ports. Serial port 1 is connected to the DDC and receives base band samples. Serial port 2 is connected to the three CODECs (encoder/decoder). Serial port 3 is not used.

3.2.4 CODECs

The three CODECs provide the audio frequency analog interface to the reciter. There are six analog input and six analog output paths. The sample rate on all paths is 25kSPS and the sampling resolution is 16 bits.

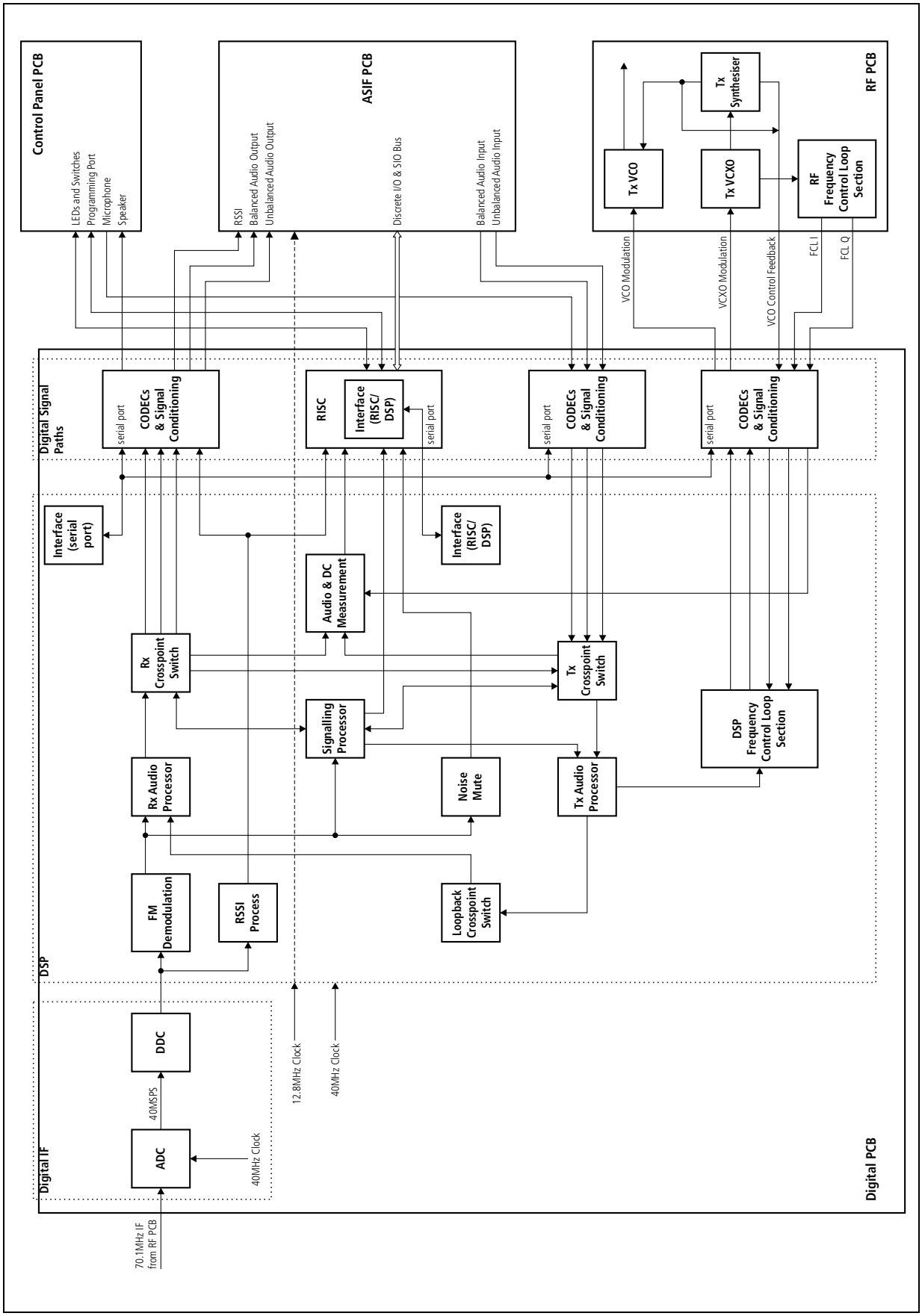
The CODEC inputs are as follows:

- two input signals from the frequency control loop (FCL)
- balanced line input
- unbalanced line input
- microphone input
- synthesizer loop control voltage.

The CODEC outputs are as follows:

- VCO voltage control line
- VCXO voltage control line
- balanced line output
- unbalanced line output
- speaker output
- RSSI voltage indicator.

Figure 3.1 Reciter Digital Circuitry Block Diagram



3.3 Reduced Instruction Set Computer (RISC)

Refer to Figure 3.2 on page 26.

3.3.1 Hardware and I/O

The RISC processor engine is a Samsung S3C3410X processor with a 40 MHz external clock. It has 4 megabytes of flash memory containing the following:

- bootloader
- application code
- DSP code
- non-volatile data
- 2 megabytes of RAM for run-time variables.

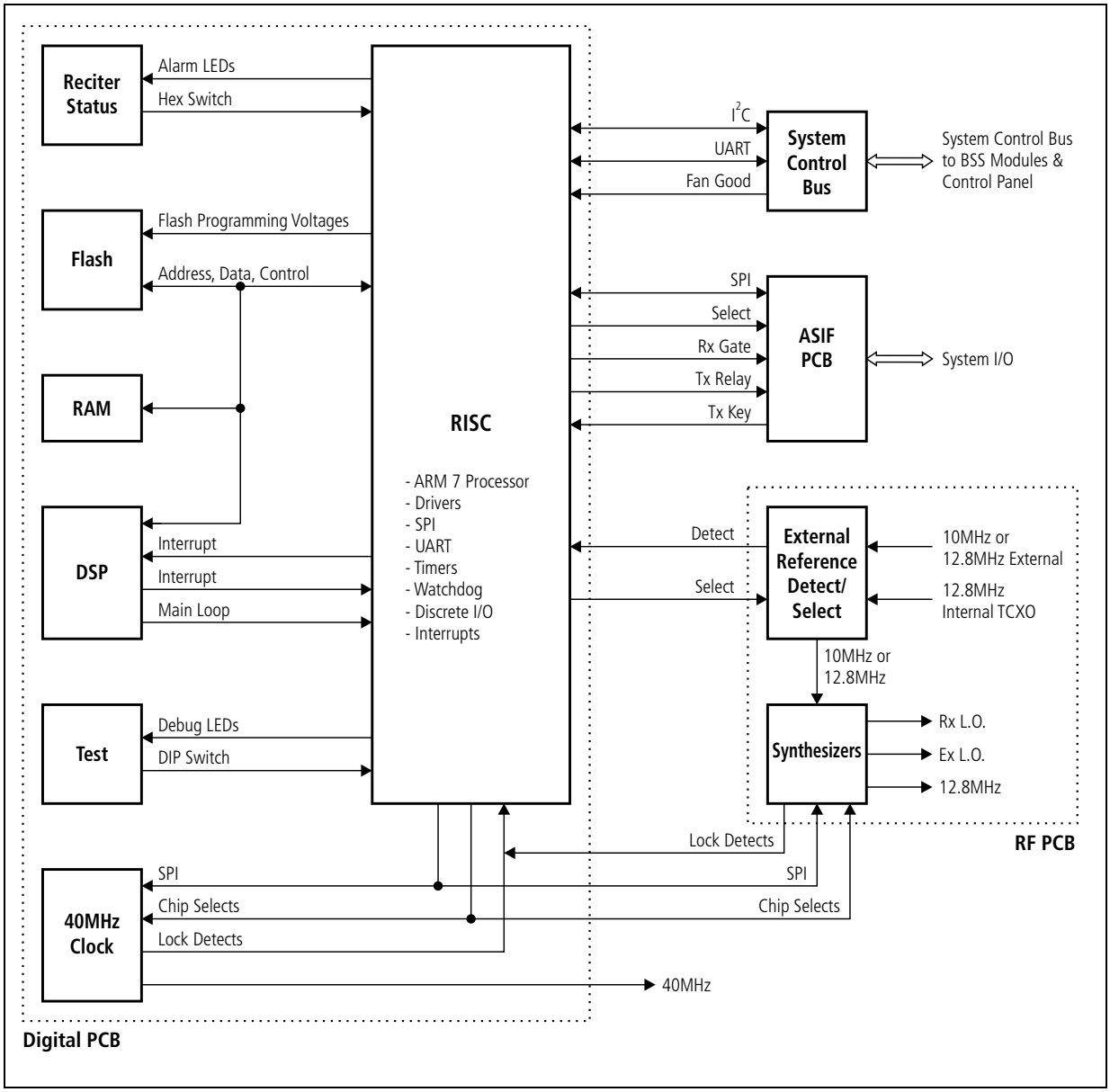
The discrete digital inputs and outputs are as follows:

- chip select signals to synthesizers
- out-of-lock signals from synthesizers
- external reference detection
- internal/external reference selection
- Rx Gate output
- Tx Relay output
- reciter hex switch
- reciter alarm LED
- DIP switch for manufacturing testing
- debug LEDs
- fan good input
- flash programming voltage control.

The RISC has the following serial interfaces:

- asynchronous serial port for communication with the CCS software and CCTM
- serial peripheral interface (SPI) for programming the synthesizers
- SPI for communication with the network PCB
- I^2C for communication with the control panel and other modules in the subrack.

Figure 3.2 Reciter RISC Functional Block Diagram



3.3.2 Responsibilities

The RISC communicates with the DSP's shared memory via a host port interface. It loads the DSP code and monitors and controls the following DSP operations:

- receive path
- transmit path
- crosspoint switches
- power supplies
- PA Key output.

The RISC controls the frequency generation subsystem. It detects an external reference source and selects internal or external reference. It also programs, and handles out-of-lock signals for, the following synthesizers:

- 12.8MHz external reference synthesizer
- 40MHz digital clock synthesizer
- receiver synthesizer
- exciter synthesizer.

The RISC communicates with the control panel via I^2C bus to:

- read the button states
- read the microphone PTT state
- control the LEDs
- turn the speaker amplifier on and off
- turn the microphone amplifier on and off.

The following signals go via the control panel for signal conditioning:

- CSS communication via the RS-232 interface
- fan-good indication (front panel fans).

Note that the volume control on the control panel is analog only and is not controlled by the RISC.

The RISC communicates with the other modules in the subrack via I^2C in order to:

- verify that they are present
- write configuration settings
- read their current status.

The RISC subsystem communicates with the network PCB via SPI to:

- set input and output gains
- mute and unmute outputs
- read digital inputs
- write digital outputs.

The Rx Gate and Tx Relay lines go via the network PCB for signal conditioning.

3.4 40MHz Digital Clock

The 40MHz synthesized digital clock is situated on the digital PCB. It is used to drive the entire digital circuitry.

The 40MHz frequency synthesizer is implemented using an Integer_N-based phase locked loop (PLL) IC. The PLL is a negative feedback loop,

which continuously monitors and maintains the 40MHz VCXO to a fixed frequency and constant phase relationship with respect to a 12.8MHz reference. The 40MHz VCXO oscillator is electrically tuned using two varactors. The oscillator output is buffered before being distributed to the digital circuitry.

4 Reference Switch

Refer to Figure 4.1 on page 31.

4.1 Synthesizer

The external reference synthesizer consists of a programmable frequency synthesizer IC, a 12.8MHz VCXO, and a stable 10MHz or 12.8MHz reference frequency supplied to the reciter externally via a BNC connector on the rear panel.

The synthesizer uses a phase-locked loop to lock the 12.8MHz VCXO to the external reference frequency. The synthesizer IC receives the divider and control information from the RISC processor via a 3-wire serial bus (clock, data and enable). When the data bits are latched in, the synthesizer processes incoming signals from the 12.8MHz VCXO feedback buffer (f_{vcxofb}) and the external reference buffer (f_{ref}).

A transistor is used as a unity gain 12.8MHz VCXO feedback buffer for the prescaler within the synthesizer IC.

The 10MHz or 12.8MHz externally supplied reference is detected, buffered and divided down to the 100kHz divider reference within the synthesizer IC. The same divider reference is maintained by dividing the 12.8MHz VCXO feedback buffered signal using the programmable dividers of the synthesizer IC. Phase lock is achieved when both divider references have the same phase and frequency content (i.e. their difference is zero or DC). This is achieved by the digital phase detector (part of the synthesizer IC), which compares both divider references and delivers an error signal. A ±1mA charge pump circuit (also part of the synthesizer IC) and the passive loop filter circuit convert this error signal to a DC voltage (0 to 3V) to tune the 12.8MHz VCXO for correction. A loop filter with a bandwidth of 180Hz further filters the VCO control line reference side bands and spurious signals.

Note The VCXO frequency increases as the control line voltage increases.

4.2 VCXO

The VCXO is implemented by using a varactor to linearly tune a 12.8MHz crystal unit over a specified frequency range. The frequency range provided will cover frequency drifts due to calibration, the temperature tolerance of

the crystal unit, and the frequency stability of the externally supplied reference.

4.3 Reference Switch

The reference switch consists of the external reference detector, the hardware switch, and the digital switch.

4.3.1 External Reference Detector

A discrete NPN dual transistor pair is used as a low level signal detector. The Syn_Ref_Det signal has a high logic level when the externally supplied signal has the correct level.

4.3.2 Hardware Switch

The hardware switch is implemented using a discrete dual transistor pair. When the switch is off (default), it powers up the internal reference 12.8MHz TCXO and shuts down the external reference 12.8MHz VCXO. When the switch is on, it powers up the external reference 12.8MHz VCXO and shuts down the internal reference 12.8MHz TCXO.

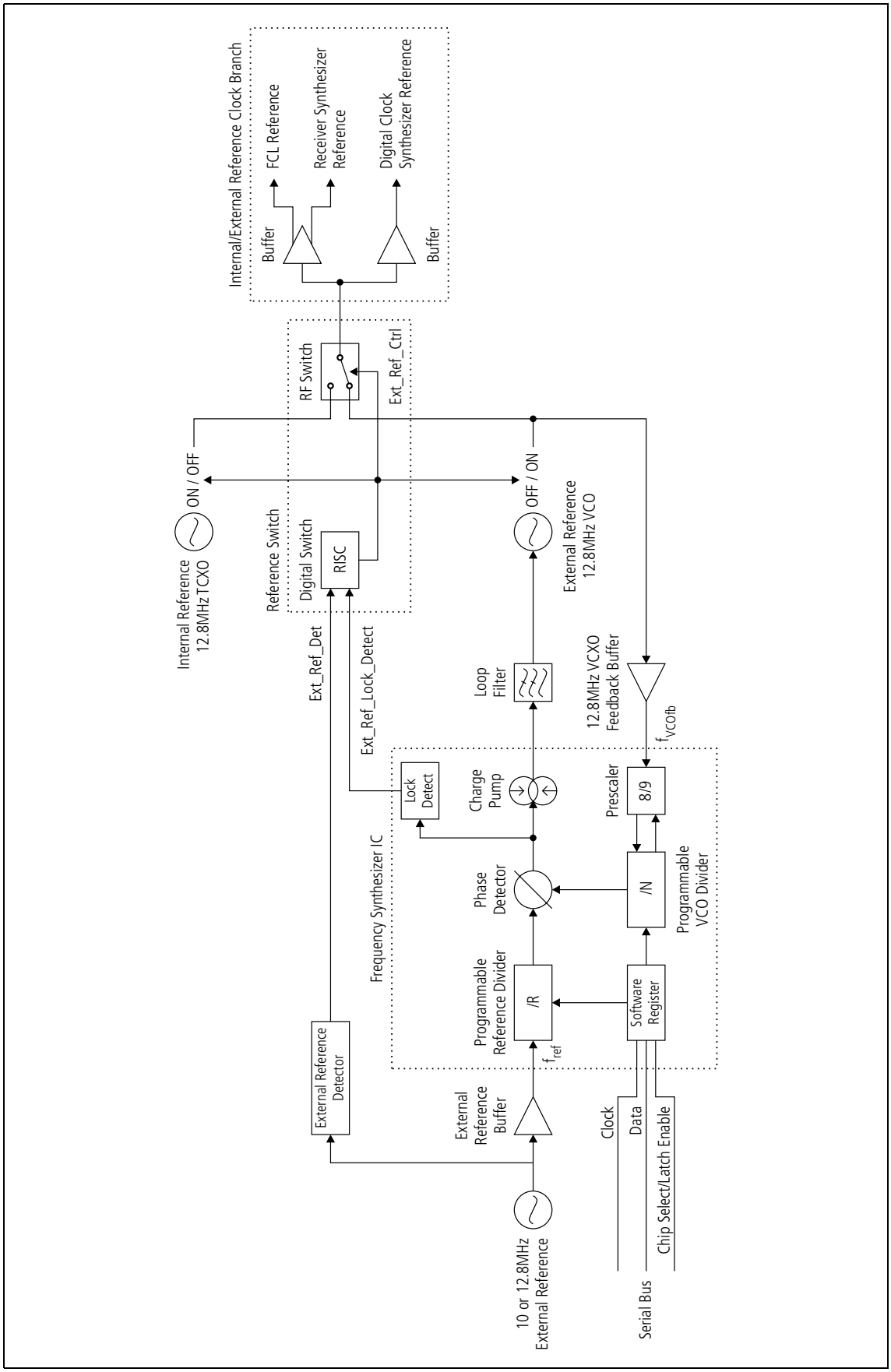
4.3.3 Digital Switch

The digital switch is controlled by the RISC, which processes the Syn_Ref_Det and Lock Detect signals from the external reference synthesizer. The RISC controls the hardware switch using the Syn_Ref_Ctrl signal. The hardware switch is on if the Syn_Ref_Det **and** Lock Detect signals have a high logic level for a set time. In all other conditions the hardware switch is off.

4.3.4 Internal/External Reference Clock Branch

A complementary emitter follower, using NPN/PNP dual transistors, forms two clock buffer branches which distribute the internal or external references to the rest of the system. The branches provide a reasonable drive level at low impedance.

Figure 4.1 Reciter External Reference Block Diagram



5 Network Circuitry

5.1 Top Level Block Diagram

A simplified block diagram of the ASIF is shown in Figure 5.1. The top-level schematic sheet (226-02056-01 sheet 1) shows a more detailed view of the main circuit blocks together with their interconnections and external connections to/from the ASIF board.

There are seven main circuit blocks:

- RISC processor
- DSP
- I/O buffers
- ethernet interface
- audio and E&M interface
- clock oscillator
- power supply

The RISC processor block (see "Risc Processor" on page 38) is the heart of the ASIF, providing the main control functions and most of the peripheral interface functions. This block also contains the main memory for the ASIF (see "Memory" on page 61), all of which is interfaced to the RISC processor. From the RISC processor block various signals are routed to the reciter via connector J101 whilst other signals are routed through the I/O buffers, the ethernet interface and the audio and E&M interface blocks to connect to the outside world.

These interfaces provide signal formatting, signal level conversion, I/O protection, etc, for the logic level signals emanating from the RISC processor. The I/O buffers block (see "I/O Buffers" on page 71) mainly handles general-purpose digital I/O to/from the RISC processor along with level conversion for an RS-232 port. Also included in this block is an analog amplifier for amplifying/buffering the RSSI output. The interface acts as a conduit for the RSSI signal from the reciter, as the ASIF does not use this signal in any way.

The ethernet interface (see "Ethernet Interface" on page 74) contains an ethernet PHY chip together with line interface components. The PHY chip incorporates logic to format the ethernet signals from the RISC processor to a suitable format for line transmission. It also includes line drivers and receivers to convert the twisted pair ethernet signals to logic levels.

The audio and E&M interface (see "Audio and E&M Interface" on page 77) is jointly controlled by the RISC processor and the DSP. The E&M signalling is connected to the RISC processor. Audio data to/from the DSP

is converted to analog signals by a CODEC chip. However, the CODEC chip configuration is controlled by the RISC processor rather than the DSP.

The DSP block (see "DSP" on page 65) contains the DSP chip, which acts as a peripheral processor to the RISC processor. The RISC processor can communicate with the DSP through a host port interface, whereby the RISC processor can access the DSP's memory as though it existed in the RISC processor's memory space. The DSP block does not contain any memory external to the DSP chip itself.

Two high-speed serial ports provide I/O capabilities for the DSP; one connects to the CODEC in the audio interface, the other connects, via J102, to the DSP on the reciter board. The RISC processor can also connect to the reciter DSP through this same high speed serial port, but this interface is not presently used in the ASIF application.

The clock oscillator block contains a clock oscillator for the RISC processor and a clock buffer to buffer the clock from the reciter board before being fed to the DSP. The power supply block contains several power convertors that convert the incoming +28V supply to the various power supply voltages required by the ASIF circuitry. The power supply block also includes the power-on reset circuitry

5.1.1 Connectors

On the rear panel of the ASIF there are three connectors for external I/O:

- DB9 connector, J103, connects to external digital I/O and a basic RS-232 serial port
- RJ45 connector, J104, connects the ethernet port
- RJ45 connector, J105, connects the 4W audio and E&M signalling port.

Although both J104 and J105 use the same type of connector, J105 is keyed to prevent its plug being accidentally inserted into J104. This prevents the potentially high voltages on the E&M lines from damaging the ethernet interface.

Along the top edge of the ASIF PCB there are two connectors for interfacing to the reciter:

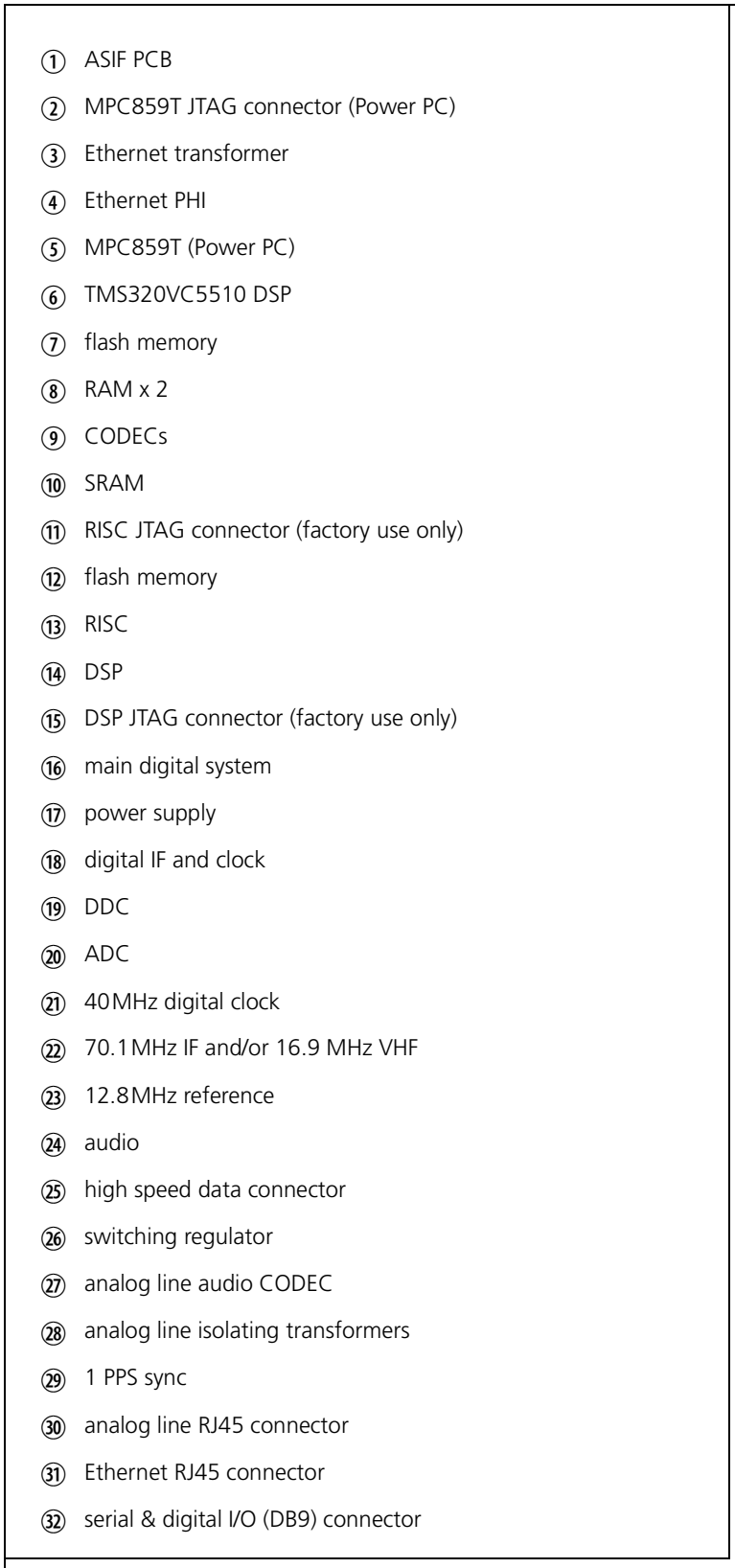
- FFC connector J101 connects power and miscellaneous digital signals from the reciter along with serial ports from the reciter RISC
- PCB connector J102 connects signals through from the reciter DSP

Two further internal connectors are used for debug and program loading purposes:

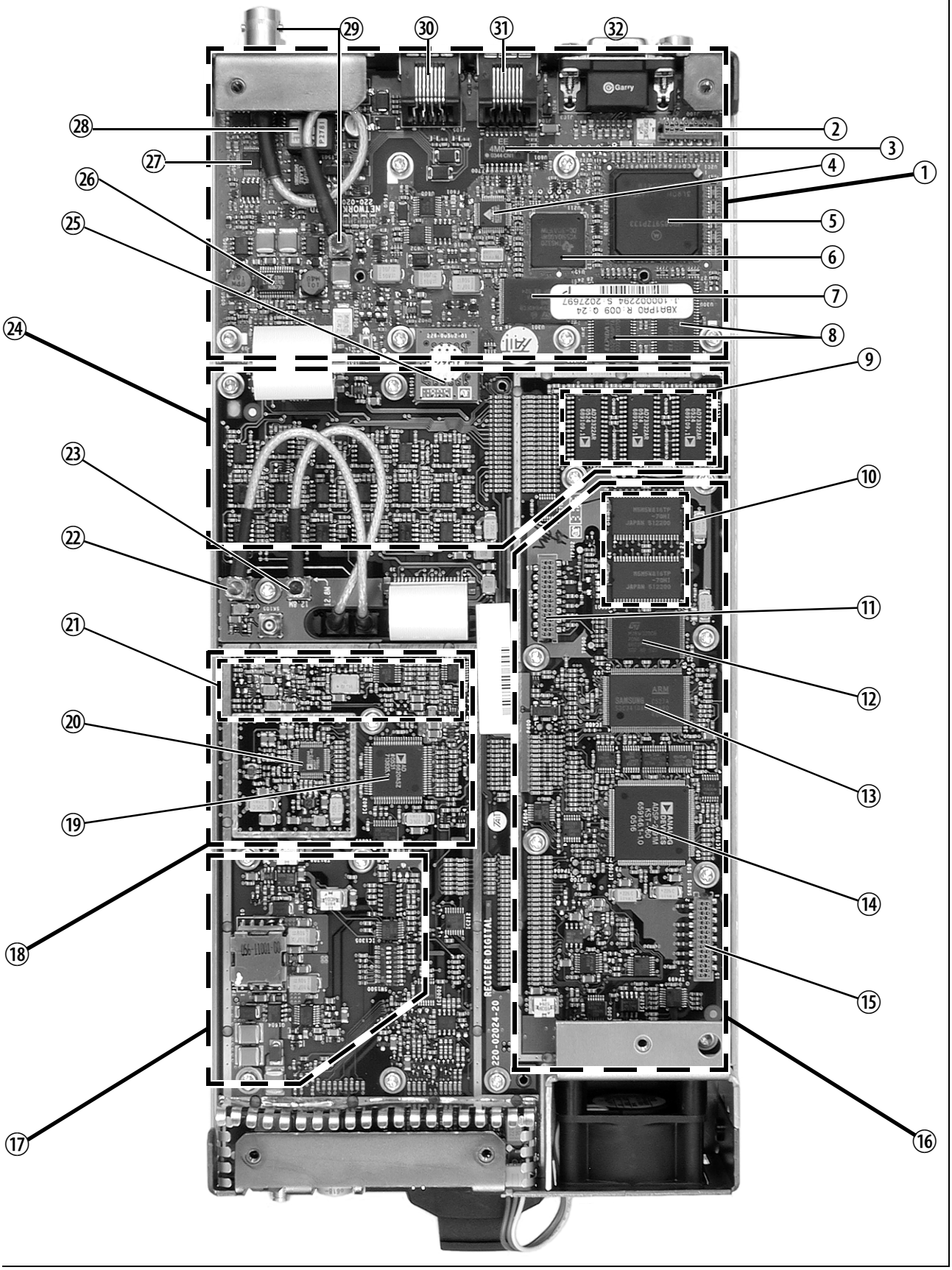
- Micro-match connector J100 is used as the debug and program loading port for the RISC processor
- Micro-match connector J106 provides a JTAG interface to the DSP for software debug purposes

Connector J100 is fitted as standard as it is used for factory loading of the initial bootloader code. JTAG connector J106 is only fitted to prototype boards used for debugging of DSP code. It cannot be fitted to production boards as it is placed on the underside of the ASIF PCB; it is not possible to fit boards equipped with J106 on to the reciter heatsink.

Figure 5.1 Identifying the Circuitry on the Digital and ASIF PCBs



① ASIF PCB
② MPC859T JTAG connector (Power PC)
③ Ethernet transformer
④ Ethernet PHI
⑤ MPC859T (Power PC)
⑥ TMS320VC5510 DSP
⑦ flash memory
⑧ RAM x 2
⑨ CODECs
⑩ SRAM
⑪ RISC JTAG connector (factory use only)
⑫ flash memory
⑬ RISC
⑭ DSP
⑮ DSP JTAG connector (factory use only)
⑯ main digital system
⑰ power supply
⑱ digital IF and clock
⑲ DDC
⑳ ADC
㉑ 40MHz digital clock
㉒ 70.1MHz IF and/or 16.9 MHz VHF
㉓ 12.8MHz reference
㉔ audio
㉕ high speed data connector
㉖ switching regulator
㉗ analog line audio CODEC
㉘ analog line isolating transformers
㉙ 1 PPS sync
㉚ analog line RJ45 connector
㉛ Ethernet RJ45 connector
㉜ serial & digital I/O (DB9) connector



5.2 Risc Processor

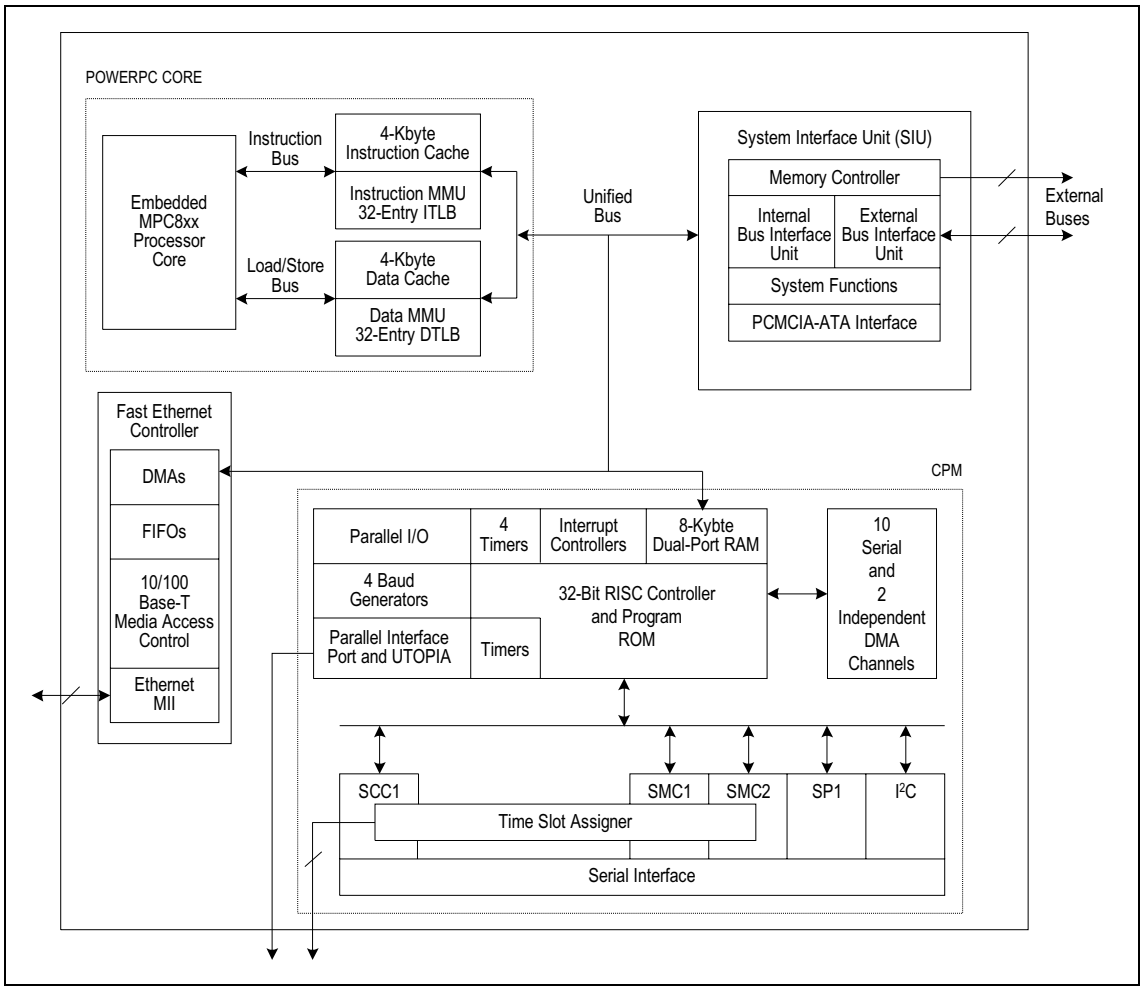
5.2.1 Risc Processor

The main processor, U201, is a PowerQUICC MPC859TPZ133, hereafter abbreviated to MPC. This device consists of a PowerPC derived RISC processor in conjunction with a micro-coded RISC based Communications Processor Module (CPM). The RISC processor runs the main application program(s) under Linux while the CPM offloads the lower level processing of various serial communications protocols.

The MPC859T is a subset member of the MPC866 PowerQUICC communications processor family and has fewer communications interfaces compared to the full function MPC866 device ie. it provides only one serial communications controller (SCC), instead of the four fitted to the MPC866.

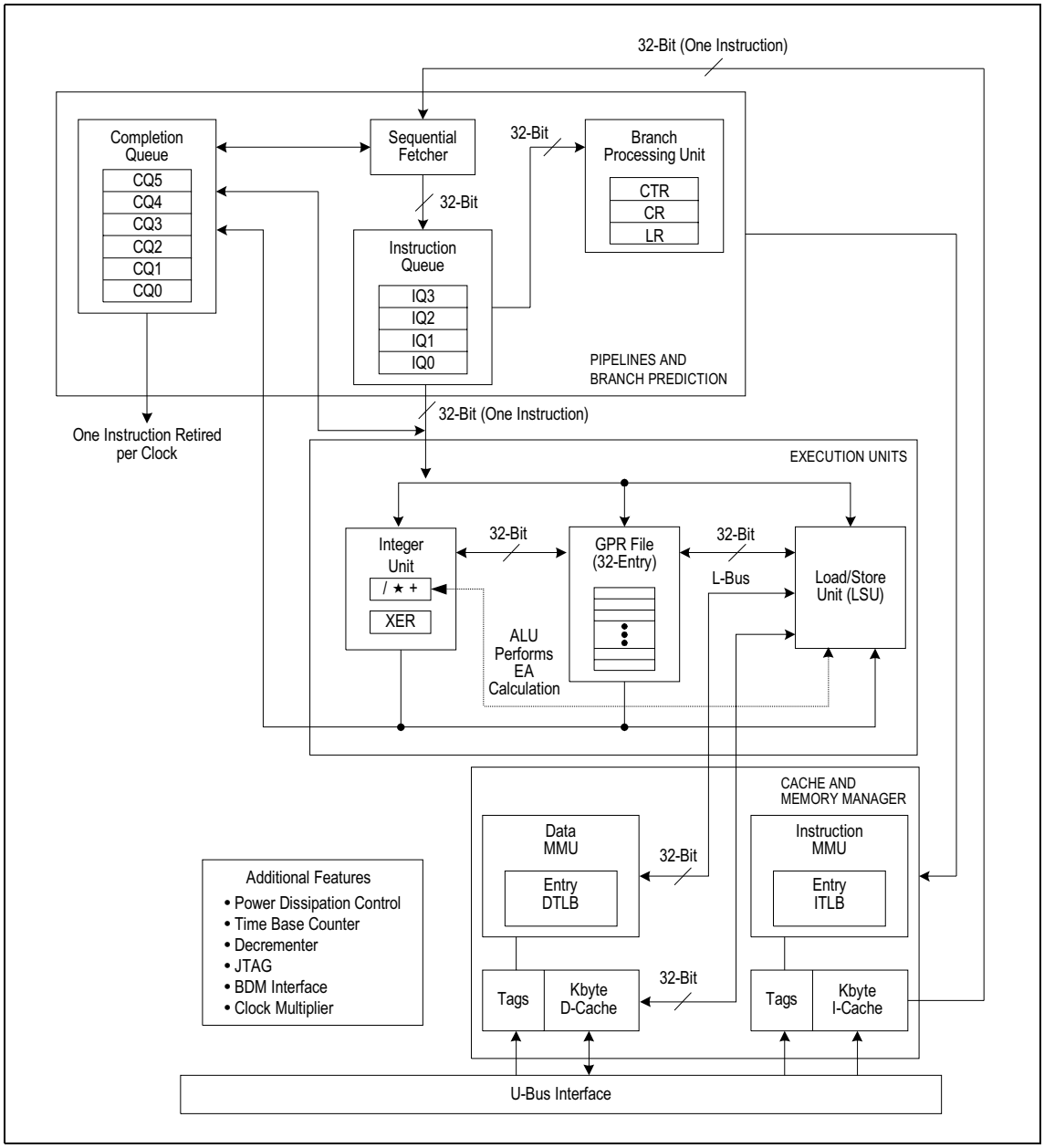
The block diagram (Figure 5.2) shows the internal structure; refer to the MPC866 data sheet (reference 1) and MPC866 user's manual (reference 2) for full details of the internal functions.

Figure 5.2 MPC859T Block Diagram



RISC Core A block diagram of the PowerPC RISC core is shown in Figure 5.3.

Figure 5.3 Processor Core Block Diagram



The RISC processor core is a PowerPC derivative implementing a full 32-bit integer CPU architecture. Its RISC (reduced instruction set computer) architecture achieves a high level of performance through having a large number (32) of internal general-purpose registers and separate integer arithmetic and load/store (LSU) execution units, which allow several operations to occur simultaneously. The arithmetic unit performs all arithmetic and logical operations on data. The LSU handles data transfers both internally to the PowerPC and to external memory and peripherals.

The performance is further enhanced by pipelining instruction fetching and execution. Instructions are pre-fetched from memory and pre-decoded to

ensure that the execution units always have a continual flow of instructions. Static branch prediction minimizes disruptions in the instruction flow through the pipelines by pre-fetching instructions following on from a program branch.

A full description of the operation and instruction set of the RISC core is outside the scope of this document. It is recommended that the MPC866 user's manual (reference 2) be consulted for comprehensive coverage of the topic.

Memory Caches and Memory Managers

Ordinarily, the fastest rate that the MPC can fetch data from external memory is one 32-bit instruction per two memory clock cycles. However, the CPU can execute two instructions per memory clock cycle since its internal clock is configured to be twice the memory clock (see "Clock Generation" on page 42 and "MPC Configuration" on page 45). Therefore, the CPU performance is restricted by the available transfer bandwidth from its program memory.

To enable the CPU to run at full speed, internal cache memory, which enables fetching of data or instructions without wait states, is provided. The MPC859T includes separate instruction and data caches of 1kwords (4kbytes) each.

The CPU implements a Harvard architecture internally, ie. there are separate instruction and data caches, each with separate data and address buses. This allows data and instruction fetches from the caches to occur simultaneously. Although the internal structure of the instruction and data caches differs, they operate in an essentially similar fashion.

Considering instruction fetches only, when the CPU fetches an instruction word and that instruction is found within the instruction cache, then it can be retrieved without delay. Should the required instruction not be in cache then the cache issues a request to the SIU (see "System Interface Unit (SIU)" on page 42) to fetch that instruction from main memory. Actually, a total of four words is fetched in a burst fetch (see "SDRAM Burst Cycles" on page 64) since the cache memory is organized in lines of four words each, which are updated together.

If there is spare space in the cache, the new instruction data is stored in the cache. Otherwise, space must be cleared in the cache to enable the newly fetched data to be retained. To accomplish this, cache entries are examined to find the oldest entry using a least-recently-used (LRU) algorithm. The oldest cache entry thus found is discarded to make way for the new data.

The MPC provides memory management support for high-end operating systems through separate instruction and data memory managers. These translate the logical address from the RISC core into a real address used to access external memory and peripherals. Separate instruction and data memory managers support the Harvard architecture of the CPU but their

outputs are combined into a single unified bus, ie. a von Neumann architecture, for external memory and peripheral accesses.

As well as address translation, the memory managers can apply protection attributes to areas of memory. The parameters for translation and protection are stored in tables in main memory. To speed up the translation process the most recently used parameters are stored in internal registers called Translation Lookaside Buffers; ITLB for the instruction memory manager and DTLB for the data memory manager.

Debug Facilities and Program Loading

The MPC provides comprehensive internal debug facilities to support the software debugging process. A description of the full functionality of the debug capabilities is outside the scope of this document; a thorough study of chapter 45 of the MPC866 user's manual (reference 2) is recommended.

The MPC debug interface can be activated directly out of reset, or upon the occurrence of one of a number of machine exceptions. Activation of debug mode out of reset requires the presence of an external debugger connected to the debug connector, J100. Without the debugger connected, the MPC operates normally and starts executing code from its program memory until a machine exception occurs. These machine exceptions can be handled internally by the interrupt service software or can be configured to start debug mode.

Once debug mode is activated, the processor core fetches its instructions from the debug interface rather than program memory. This allows the processor registers and memory to be examined, or changed, and code to be downloaded by the external debug tool. This download mode is also used for transferring the bootloader software into the external flash EPROM on a newly manufactured board.

If debug mode has been entered as a result of an exception, the cause of that exception is indicated in the debug interface registers. The debug interface also allows the setting up of breakpoints and watch-points. The watch-point and breakpoint comparators can detect accesses to defined address(es) or force a processor exception (interrupt) when a certain address is accessed, even when the MPC is operating at full speed. Watch-point flags are externally visible on test points TP202-TP203 and TP207-TP208 for triggering logic analyzers or oscilloscopes.

The external connection to the debug interface is through a simple full-duplex clocked serial interface. Data is clocked into the debug interface on the Development Serial Data In (DSDI) pin; data is clocked out on the Development Serial Data Out (DSDO) pin. Data is clocked in on the rising edge of the Development Serial Clock (DSCK) and out on the falling edge of DSCK. The state of DSCK during a processor reset determines whether debug mode is started out of reset. These serial interface pins are brought out to connector J100 along with the reset signals ($\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$) and the CPU status pins (VFLS0, VFLS1).

The MPC also supports JTAG mode for board testing, but this is not implemented on the ASIF due to lack of space for another connector. Basically, a JTAG port provides access to all the MPC's pins so that checks may be made for continuity, shorts, etc. Unlike the DSP (see "Processor Core" on page 66), the JTAG port is not used for program debugging on the MPC.

5.2.2 System Interface Unit (SIU)

The SIU ties together the MPC's internal and external bus interfaces and provides ancillary services to the RISC core. These include clock generation, timer functions, system configuration, interrupt control and the PCMCIA interface.

Clock Generation

To achieve high performance the MPC requires a high-frequency clock. This high-frequency clock is generated internally to the MPC by multiplying up a relatively low-frequency reference clock input, using an internal phase-locked loop (PLL) to minimize EMC problems. The input reference clock (EXTCLK) can be multiplied by various ratios with the proviso that the final PLL operating frequency must lie in the range 160MHz to 266MHz.

The CPU clock defaults to the PLL clock divided by 2, although higher division ratios are available where it is desired to run the CPU at a lower clock frequency to save power. Other clocks for peripheral circuitry are derived by independent dividers from the PLL clock so that the peripheral clocks remain constant, even if the CPU clock is reduced for lower power operation.

The multiplication ratio from reference frequency to PLL frequency is set by programming several PLL registers to give multipliers that are a ratio of two integers. In the ASIF, these registers are set for an overall multiplication ratio of 9 8/13, giving an MPC clock of 125MHz from the 13MHz reference clock (see "Clock Oscillator" on page 81).

Prior to the program running and being able to set up the PLL registers, default values are loaded into these registers to enable MPC operation. The default values are determined by the MODCK[0..1] inputs (see "MPC Reset" on page 44 and Table 5.3). Once the MPC program is up and running, it reprograms the PLL registers to their final values.

Time Bases and Watchdog

The PowerPC architecture includes several supplementary timer functions to provide hardware and software monitoring and operating system support:

- Bus monitor
- Software watchdog timer
- Periodic Interrupt Timer
- Time base counter
- Decrementer

The bus monitor timer monitors the duration of bus cycles to ensure that they are terminated within a reasonable time. If the timer expires, it asserts the $\overline{\text{TEA}}$ signal (see "MPC Bus Cycles" on page 48) to terminate the bus cycle with an error condition. The bus monitor time-out period is programmable up to 2040 bus clocks ie. approximately 32.6us at a 62.5 MHz bus clock.

The software watchdog timer provides a means of terminating a runaway program. If the watchdog is not serviced by periodically by writing specific data patterns to its service register, it eventually times out and issues a reset or a non-maskable interrupt (NMI). The watchdog timer has a programmable16-bit down counter, which is clocked from a divide-by-2048 prescaler from the main system clock. Therefore, with a 125 MHz system clock, the watchdog time-out periods can range from approximately 16us through to approximately 1s.

The periodic interrupt timer (PIT), decrementer and time base are 16, 32 and 64-bit counters respectively. They can be used to generate interrupts at specific times and are mainly used for operating system timing functions.

Interrupts

Four of the eight levels of external interrupt inputs available on the MPC are used in the ASIF, as detailed in Table 5.1. All but $\overline{\text{IRQ0}}$ can be masked under software control to ignore that interrupt source. The pin for $\overline{\text{IRQ7}}$ is utilized as a clock input for the MII (see "Media Independent Interface (MII)" on page 76); therefore $\overline{\text{IRQ7}}$ must be masked to avoid numerous spurious interrupts.

Table 5.1 MPC Interrupt Sources

Interrupt Input	Priority	Type	Source
$\overline{\text{IRQ0}}$	Highest	Non-maskable	not used
$\overline{\text{IRQ1}}$		Maskable	1 PPS
$\overline{\text{IRQ2}}$		Maskable	not used
$\overline{\text{IRQ3}}$		Maskable	DSP host port
$\overline{\text{IRQ4}}$		Maskable	Ethernet PHY
$\overline{\text{IRQ5}}$		Maskable	not used
$\overline{\text{IRQ6}}$		Maskable	E-lead
$\overline{\text{IRQ7}}$	Lowest	Maskable	not used

All interrupt inputs are active low and can be configured to be either edge or level sensitive. The priority of the external interrupts is fixed, ie. a higher priority interrupt request service routine cannot be interrupted by a lower priority interrupt request. Interrupts from internal sources are combined and prioritized along with external interrupts (see "Interrupt Controller" on page 55).

Aside from the external interrupts, the interrupt controller also combines and prioritizes interrupts from internal sources including the:

- software watchdog timer
- PCMCIA interface
- communications processor (see "Interrupt Controller" on page 55)

PCMCIA Interface

The MPC incorporates logic to control the interface to two PCMCIA card sockets. This is not used in the ASIF but the pins (IP_A[0..7]), normally used for sensing the PCMCIA card status, are used for sensing the general-purpose digital inputs (see "Parallel Ports" on page 59 and "General-purpose Digital Inputs" on page 72). These pins feature change-of-state sensing, generating an interrupt on a change of pin state. This allows the software to respond quickly to changes without the high overhead of continuous polling.

5.2.3 RISC Reset and Configuration

MPC Reset

The MPC supports several levels of resets that can be initiated internally to the MPC or driven by external devices. The different levels of resets are primarily used to enable software debugging without disturbing the internal state of some parts of the MPC. In particular, a soft reset retains the major MPC system configuration and maintains the memory controller refresh operation (see "SDRAM Refresh Cycles" on page 64), so that the dynamic memory contents are not lost.

The sources of reset used in the ASIF and their effects are detailed in Table 5.2.

Table 5.2 Reset Responses

Reset source	PLL reset	System config reset	Clock module reset	$\overline{\text{HRESET}}$ driven	Debug port config	Other internal logic reset	$\overline{\text{SRESET}}$ driven
Power-on reset	Y	Y	Y	Y	Y	Y	Y
Software watchdog, debug port hard reset	N	Y	Y	Y	Y	Y	Y
Debug port soft reset	N	N	N	N	Y	Y	Y

On power up the MPC's $\overline{\text{PORESET}}$ input is taken low by the power supply circuitry (see "Power-on Reset" on page 85). In response, the MPC drives its hard reset ($\overline{\text{HRESET}}$) and soft reset ($\overline{\text{SRESET}}$) outputs low, resetting any external circuitry connected to them.

When $\overline{\text{PORESET}}$ is released the MPC latches the state of the MODCK1 and MODCK2 pins; these provide the initial settings for the clock generator PLL in accordance with Table 5.3.

Table 5.3 Power-on Reset PLL Configuration

MODCK[1..2]	Reference clock source	System frequency
00	Internal crystal oscillator	4 x oscillator clock
01	Internal crystal oscillator	7.5 x oscillator clock
10	External clock source	1:1 mode
11	External clock source	7.5 x external clock

Pull-up resistors R213 on MODCK1 and R214 on MODCK2 select the 7.5x clock mode so that the CPU clock is initially operated at 7.5 times the 13MHz reference clock (see "Clock Oscillator" on page 81) ie. 97.5MHz. An optional pull-down resistor, R215, is provided so that the 1:1 clock mode can be selected if reference clocks higher than approximately 17MHz are used. There is no provision for selecting the internal MPC crystal oscillator, which is not used in the ASIF.

Once the $\overline{\text{PORESET}}$ input is negated and the PLL (see "Clock Generation" on page 42) has stabilized, the $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ lines remain asserted for 512 clock cycles, after which the configuration set-up (see "MPC Configuration" on page 45) proceeds.

The $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ lines are bi-directional open-collector, which allows the MPC to sense a reset signal driven by external open-collector devices. In the ASIF, this feature is used only for the BDM debug port, connected to J100 (see "Debug Facilities and Program Loading" on page 41). Pull-up resistors R201 and R203 ensure correct high logic levels when no device is asserting $\overline{\text{HRESET}}$ or $\overline{\text{SRESET}}$.

MPC Configuration

On startup there are several configuration options for the MPC that need to be set so that it can boot up as well as enable the pins supporting the debug interface. The MPC obtains these settings by latching the state of the data bus pins when $\overline{\text{HRESET}}$ transitions high, but only if the $\overline{\text{RSTCONF}}$ input pin is taken low. Otherwise, the default configuration setting of all zeroes is applied.

With $\overline{\text{RSTCONF}}$ low, the configuration register is still set to its default all-zeros condition, unless individual data bus line(s) are driven high by external circuitry, since the MPC enables internal pull-down resistors on its data bus when $\overline{\text{HRESET}}$ is asserted. Four tri-state buffers, U200, U205, U210 and U211, drive selected data bus lines high while $\overline{\text{HRESET}}$ is active, giving the configuration settings shown in Table 5.4.

Table 5.4 Boot Configuration Settings

External Data Bus Pins Driven High	MPC Configuration Register Bits		Operating Mode
	Name	Setting	
	EARB	0	External arbitration disabled
	IIP	0	Initial interrupt prefix
	BBE	0	Boot burst disabled
	BDIS	0	Boot is enabled for device selected by CS0
d17	BPS	01	Boot port device size set to 16 bits
	ISB	00	Base address on internal memory space is set to 0x00000000
d21, d22	DGBGC	11	CPU debug status signals output on port IB_B[0..7]
	DBPC	00	BDM debug port functions enabled
d27	EBDF	01	Memory clock output is 1/2 internal clock speed
	CLES	0	Big Endian mode

Note The bits set to zero in the above table are obtained from the data bus pull-downs. The external data bus bit designations are normal numbering order as opposed to the PowerPC reverse numbering order. (See "Terminology" on page 6.)

5.2.4 RISC External Bus Interface

The MPC has a single, unified bus structure for external data, code and peripheral accesses, ie. it does not support the Harvard architecture externally. The address and data buses are not multiplexed together, but different address signals may be multiplexed onto the address pins for interfacing to dynamic memory devices (see "Address Multiplexing and Command Codes" on page 63)

MPC External Data Bus

Note The numbering of the data bus lines on the schematic follows normal industry convention, ie. the lsb is D0, rather than the PowerPC convention with D31 being the lsb. The transition from PowerPC numbering order to normal numbering order occurs at the MPC external pins, ie. MPC D31 is connected to data bus D0, MPC D30 is connected to D1, and so on.

The MPC's external data bus is 32 bits wide. Normally, the MPC attempts to transfer data as 32-bit words, however, it can transfer data to/from 8-bit

or 16-bit devices with multiple read or write cycles. The transfer size is dynamically allocated by the memory controller (see "Memory Controllers" on page 49) and is encoded on the transfer size output pins, TSIZ[0..1], as per Table 5.5.

Table 5.5 Transfer Size Encoding

TSIZ[0..1]		Port Size
0	0	32-bit word
0	1	8-bit byte
1	0	16-bit half-word
1	1	reserved

When writing to memory the MPC always writes 32-bit words, even when writing an 8-bit or 16-bit value. To prevent writes to spurious byte or half-word locations, the write enable signals, $\overline{WE[0..3]}$, and the byte select signals, $\overline{BS[0..3]}$, select the relevant byte(s) in a word for accesses controlled by the GPCM (see "General-Purpose Chip Select Machine" on page 50) and UPMA (see "User-Programmable Machines" on page 51) respectively.

The MPC architecture includes provision for a parity bit to be attached to each byte and for these parity bits to be output/checked on each memory cycle. Parity checking is not used in the ASIF.

MPC External Address Bus

Note The numbering of the address bus lines on the schematic follows the normal industry convention, ie. the lsb is A0, rather than the PowerPC convention with A31 being the lsb. The transition from PowerPC numbering order to normal numbering order occurs at the MPC pins, ie. MPC A31 is connected to address bus A0, MPC A30 is connected to A1, and so on.

The MPC's external address bus is 32 bits wide supporting an address space of 4Gb. Only the lower order 27 bits are used in the ASIF application to cover the addressing requirements of the largest memory or peripheral device. The chip select decoding is handled internally to the MPC using a full 32-bit address decode so that devices do not appear at multiple locations in the memory map due to incomplete address decoding.

The lower order addresses, A0 - A13, are multiplexed when accessing the SDRAM (see "Address Multiplexing and Command Codes" on page 63). As this multiplexing occurs at a relatively high speed, series damping resistors are fitted to these lines to improve the signal quality. The resistors reduce the signal rise time slightly and absorb any signals reflected back from the memory device pins.

MPC Bus Cycles

The MPC is capable of arbitrating with other external bus servers for control of the address and data buses using the Bus Request ($\overline{BR}$), Bus Grant ($\overline{BG}$) and Bus Busy ($\overline{BB}$) pins. External bus servers are not used in the ASIF design, so the MPC is configured (see "MPC Configuration" on page 45) for internal arbitration, and the bus arbitration pins are pulled up to their inactive high state.

Assuming that the MPC has obtained ownership of the bus, it starts a bus cycle by outputting the address and the transfer attributes detailed in Table 5.6. The transfer start signal ($\overline{TS}$) is asserted to indicate the start of a bus cycle.

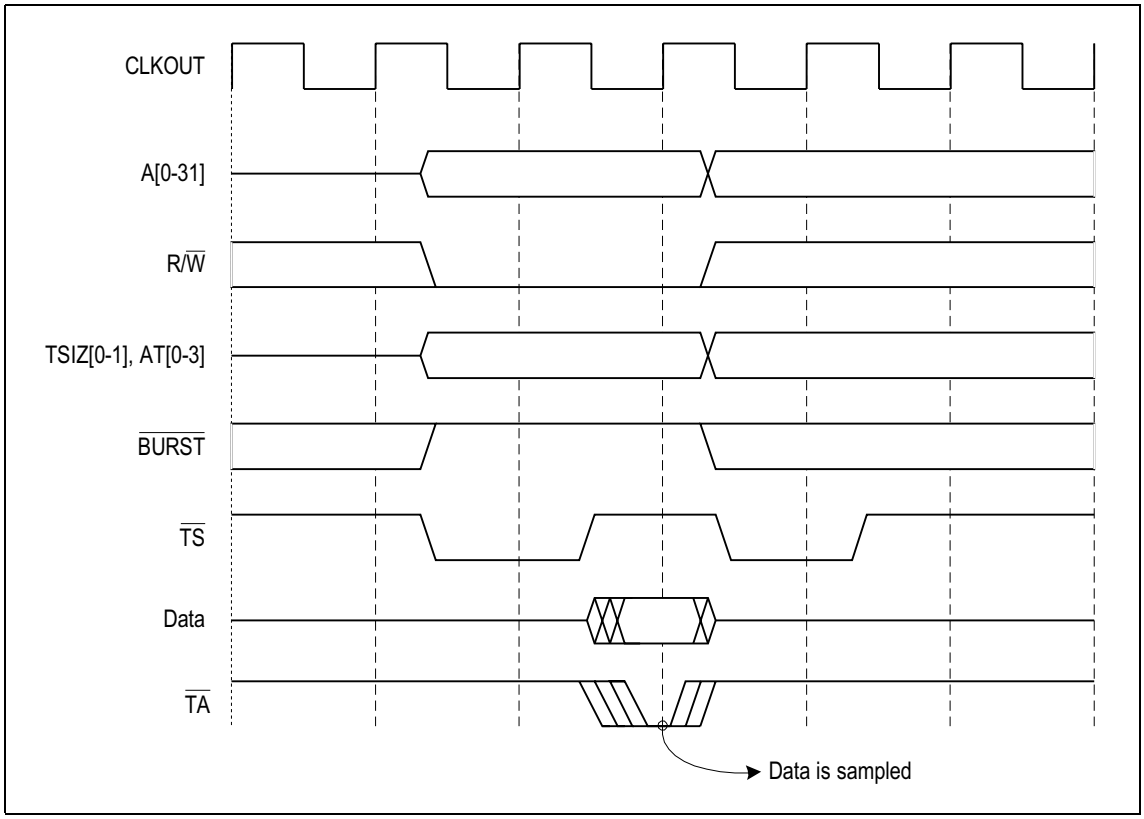
Table 5.6 Bus Cycle Transfer Attributes

Transfer Attribute	Function
RD/$\overline{WR}$	Read/write cycle
AT[0..3]	Address type modifier 0: Core/CPM access Address type modifier 1: User/supervisor access Address type modifier 2: Instruction/Data Address type modifier 3: Reservation/Program Trace
TSIZ[0..1]	Transfer size (see Table 5.5)
$\overline{STS}$	Special transfer start: used for debugging purposes
$\overline{BURST}$	Burst transfer: indicates memory cycle is a burst operation (see "SDRAM Burst Cycles" on page 64)
$\overline{BDIP}$	Burst data in progress: indicates another data transfer is expected

Except for the RD/$\overline{WR}$ line, none of the above transfer attributes are used in the ASIF external memory logic, but they may be used internally by the memory controllers (see "Memory Controllers" on page 49) to determine the cycle type. Some are available on test points to facilitate hardware and program debugging.

When the memory or peripheral devices has output/input the data to/from the bus, it tells the MPC to terminate the bus cycle by asserting the transfer acknowledge signal ($\overline{TA}$). For devices that do not have a suitable transfer acknowledge signal, this can be provided internally by the relevant memory controller (see "Memory Controllers" on page 49). The sequence of operations for a single (ie. non-burst) bus write cycle is shown in Figure 5.4.

Figure 5.4 MPC External Bus Cycle Sequence



In the event that a bus cycle is not successfully completed, either the retry ($\overline{\text{RETRY}}$) signal can be asserted to re-run the bus cycle, or the transfer error acknowledge ($\overline{\text{TEA}}$) signal can be asserted to cancel the bus cycle. Since neither of these signals is used in the ASIF, there exists a possibility that the MPC will wait forever for a bus cycle to complete. To catch any such occurrences, the bus monitor (see "Time Bases and Watchdog" on page 42) terminates excessively long bus cycles.

Normal bus operations initiated by the MPC are synchronous to the memory clock, CLKOUT, ie. all control outputs are timed from the rising edge of the clock. Similarly, all control inputs must be set up at a suitable time, prior to the rising edge of CLKOUT, to be recognized during the next clock cycle.

Memory Controllers

The MPC implements a glueless interface to standard memory types and peripherals through three programmable memory access controllers; the General-purpose Chip Select Machine (GPCM) and the User-Programmable Machines (UPMA and UPMB). UPMA and UPMB are architecturally identical. A full description of the operation of these memory controllers is beyond the scope of this document; chapter 15 of the MPC866 user's manual (reference 2) should be consulted for full details.

Between them, these controllers can generate the necessary control signals to interface with parallel bus devices such as:

- asynchronous SRAM
- synchronous SRAM
- synchronous burst SRAM
- asynchronous flash EPROM
- synchronous burst flash EPROM
- standard EPROM
- standard DRAM
- fast page DRAM
- EDO DRAM
- SDRAM
- most types of bus interfaced peripheral chips, when connected as memory mapped devices

UPMA is used to control accesses to SDRAM while the GPCM is used to control accesses to the flash EPROM and the DSP chip, which is classified as a bus interfaced peripheral. UPMB is not used in the ASIF design.

Each chip select output, $\overline{CS[0..7]}$, has a memory controller assigned to it (see Table 5.7) according to the requirements of the device selected by that chip select. The assignment is controlled via internal MPC registers, which also allocate a particular address range to a device and sets other parameters such as address type, bus width, parity enable and write protect.

Table 5.7 Chip Select Allocation

Chip Select Output	Memory Controller	Device
$\overline{CS0}$	GPCM	Flash EPROM
$\overline{CS1}$	UPMA	SDRAM
$\overline{CS2}$	GPCM	DSP
$\overline{CS3}$	GPCM	software test strobe
$\overline{CS4}$	none	none
$\overline{CS5}$	none	none
$\overline{CS6}$	none	none
$\overline{CS7}$	none	none

General-Purpose Chip Select Machine

The general-purpose chip select machine (GPCM) is normally used for controlling simple asynchronous memories such as the flash EPROM. It is also used for controlling the accesses to the DSP host port (see "Host Port Interface (HPI)" on page 69) and a software strobe output. Hence, the GPCM is assigned to handle the $\overline{CS0}$, $\overline{CS2}$ and $\overline{CS3}$ chip select lines. The GPCM also controls the write enable ($\overline{WE0}$) and read enable ($\overline{OE}$) strobes to the flash EPROM and DSP.

On initial boot up the MPC must obtain its program code from the flash EPROM, before the GPCM has been initialized by the MPC, to access that flash EPROM. To overcome this problem, $\overline{CS0}$ has a special default configuration after reset: it is active for the entire external address space of the MPC and inserts the maximum number of wait states per access.

Therefore, an EPROM connected to $\overline{CS0}$ is selected, regardless of its position in the memory map, and it can have an access time of up to 30 wait states, ie. 480ns at a 62.5MHz memory clock. Once the MPC program is loaded, it can reprogram the GPCM configuration for $\overline{CS0}$ to assign the flash EPROM's normal address location and reduce the wait states to 5 clock cycles for speedier access.

For $\overline{CS0}$ the GPCM is programmed to assert the internal $\overline{TA}$ signal (see "MPC Bus Cycles" on page 48) to terminate the bus cycle after the wait states have expired. Software strobe output $\overline{CS3}$ also utilizes the internal $\overline{TA}$ signal.

However, the handling of $\overline{CS2}$ differs; this is configured to be terminated by the external $\overline{TA}$ signal. Usually, a $\overline{CS2}$ bus cycle is terminated by the external signal, as applied by tri-state buffer U212. This buffer is controlled by the HRDY signal from the DSP, signalling the completion of a HPI access cycle (see "Host Port Interface (HPI)" on page 69). In the event that the HRDY signal does not terminate the bus cycle within approximately 32us, the bus cycle times out and is terminated by the bus monitor (see "Time Bases and Watchdog" on page 42).

User-Programmable Machines

UPMA is used for controlling accesses to, and generating the control signals for, the SDRAM devices. As well as chip select $\overline{CS1}$, UPMA controls the byte select lines, $\overline{BS[0..3]}$. The general-purpose memory control lines, $\overline{GPLA0}$, $\overline{GPLA1}$, $\overline{GPLA2}$ and $\overline{GPLA3}$, which correspond to the SDRAM A10, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ inputs respectively (see "SDRAM Control Inputs" on page 62), are also generated by UPMA. The UPM also controls multiplexing of the row and column addresses (see "Address Multiplexing and Command Codes" on page 63) onto the MPC's lower order address outputs.

The signal types and timing of the general-purpose memory control lines are fully programmable, enabling the UPM to handle a wide variety of memory and peripheral types. The configuration of these signals is determined by a pattern stored in a small 64-word RAM in each UPM. The RAM must be programmed with the appropriate data patterns by the user program before any access can be made to memory controlled by a UPM.

Each location in this RAM holds the data pattern to be sequentially output on the general-purpose lines during a memory cycle. In response to a memory cycle request, a counter is set to the appropriate location in RAM; the RAM is subdivided into sections corresponding to the different types of memory requests:

- single word read cycle request

- burst read cycle request
- single word write cycle request
- burst write cycle request
- periodic timer request
- exception condition request

The counter continues indexing through the RAM until it encounters a LAST codeword, signifying the end of a pattern, or a LOOP codeword to repeat part of a pattern. Normally, the RAM pattern controls the assertion of $\overline{TA}$ to terminate the memory cycle and reset the control lines to their idle state.

The signals output for a single-word read and write accesses are detailed in "SDRAM Read and Write Cycles" on page 64, while the burst read and write cycles are detailed in "SDRAM Burst Cycles" on page 64.
The periodic timer request is used for initiating refresh cycles (see "SDRAM Refresh Cycles" on page 64). Each UPM incorporates a timer, which can be programmed to initiate regular requests for running a memory refresh cycle at the required rate.

The exception condition request is only used in the case where a memory cycle is terminated abnormally by a $\overline{TEA}$ (see "MPC Bus Cycles" on page 48) or bus monitor time out (see "Time Bases and Watchdog" on page 42). Its function is to allow the UPM to 'clean up' after an incomplete memory cycle, ie. it restores all the control signals to their idle states ready for the next memory cycle.

5.2.5 RISC Peripherals

Communications Processor Interface

Communication between RISC and CPM takes place through an internal 8k-byte dual-port RAM or through a CPM command register.

The RISC defines buffer descriptors and parameters in the dual-port RAM to specify the required serial communications protocols. A command register is then used to instruct the CPM to initialize its parameters and to start and stop communications on a particular channel.

The CPM also incorporates a DMA controller (see "CPM Serial Direct Memory Access (SDMA)" on page 54) so that it can directly transfer data to or from the RISC's main memory space.

Fast Ethernet Controller

Note

A full description of ethernet (more properly described as Carrier Sense Multiple Access with Collision Detection, CSMA/CD) operation is outside the scope of this document. For those unfamiliar with ethernet principles, it is recommended that a standard text (reference 21) be consulted.

Independently of the serial communications facilities provided by the CPM, a fast ethernet controller (FEC) is provided for either 100Mbps (100BaseT) or 10Mbps (10BaseT) ethernet. Both half-duplex and full-duplex modes are supported.

The FEC implements only the media access controller (MAC) functions of an ethernet interface. It requires external interface hardware to implement the physical layer connection. The FEC connects to this ethernet physical layer interface (PHY) device (see "Ethernet Physical Interface" on page 74) using a media-independent interface (MII) bus (see "Media Independent Interface (MII)" on page 76). It also supports a 7-wire interface to connect to older 10Mbps physical interface devices, but this is not used in the ASIF. For test purposes, the FEC can perform an internal loopback function bypassing the PHY, or it can instruct the PHY to perform an external loopback function.

For ethernet transmissions, the MPC will typically set up the data in a transmit buffer location in external memory. The location of this buffer is made known to the FEC via a transmit buffer descriptor (BD), also describing the length of the data packet, its destination address and other relevant settings. Thereafter, the FEC handles the necessary transmit operations, eg. data frame formatting, preamble generation, data transmission and appending CRC information, without further MPC intervention. In the event of a transmit collision occurring, the FEC can handle the transmit retries independently of the MPC.

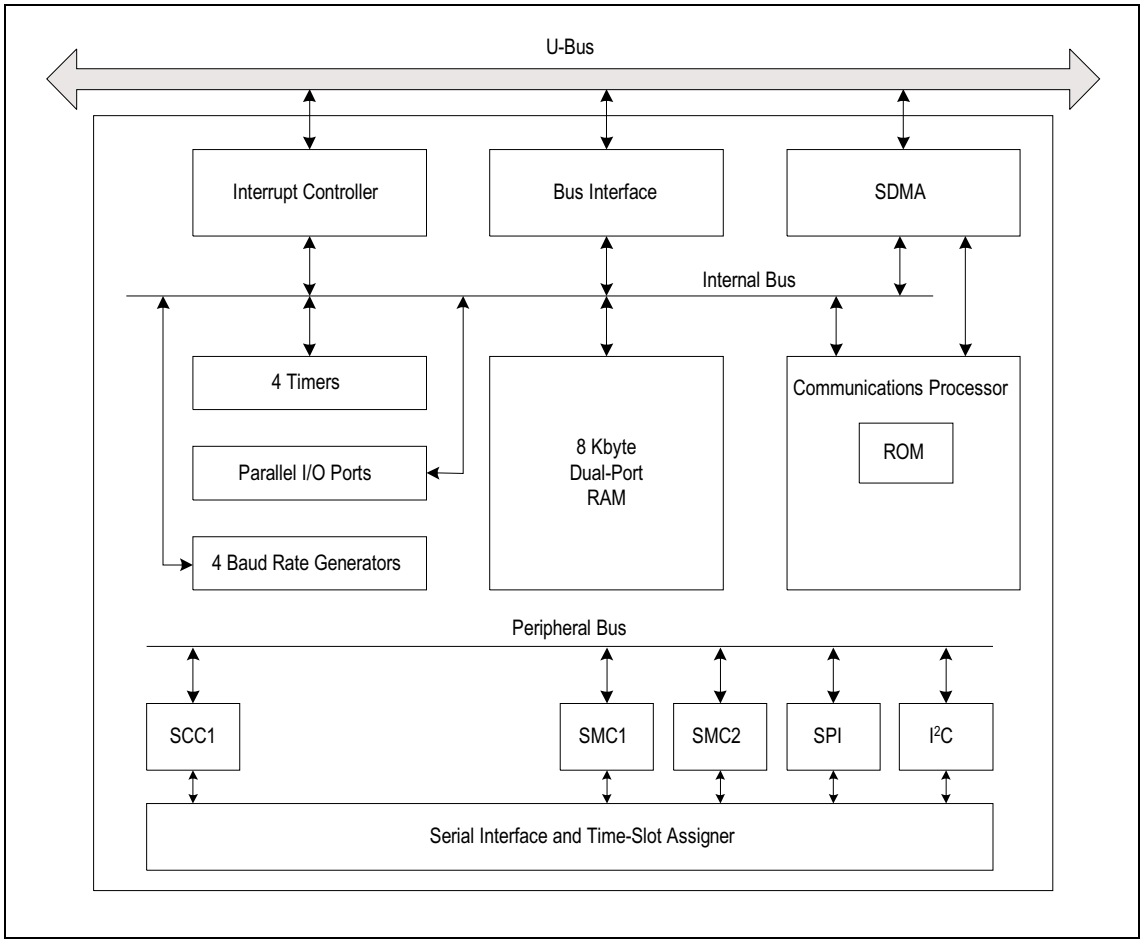
Similarly for ethernet reception, the FEC handles preamble detection, frame detection, address recognition, data reception and CRC checking. Received data is placed in a memory buffer according to the receive buffer descriptor, which is also records status information for the received frame. To minimize loading on the MPC, the FEC employs several address filtering methods to ignore ethernet frames that are not addressed to it.

Data transfers to/from the main memory buffers take place using DMA (see "CPM Serial Direct Memory Access (SDMA)" on page 54). FIFOs within the FEC allow the DMA to take place in bursts, minimizing the memory bandwidth required.

5.2.6 Communications Processor

The CPM supports many varieties of serial interface protocols through microcode executing from an internal ROM. It performs lower level control of serial functions, taking much of the interface and protocol management workload away from the main RISC CPU. A block diagram of the CPM is shown in Figure 5.5. Reference should be made to Part V of the MPC866 user's manual (reference 2) for a detailed description of the CPM's capabilities.

Figure 5.5 Communications Processor Block Diagram



CPM Serial Direct Memory Access (SDMA)

To avoid the need for the MPC software to transfer large blocks of data to/from the CPM, a DMA controller is implemented in the CPM. This DMA controller can transfer to/from external memory and to/from the CPM's dual port RAM.

The DMA hardware supports two DMA channels, but the CPM software expands this to 16 virtual DMA channels with dedicated channels assigned to each serial device, eg. SCC, and SMC. A further two virtual DMA channels are assigned for independent DMA to/from devices external to the MPC. This function is not used in the ASIF.

Timers and Baud Rate Generators

The CPM incorporates four 16-bit timers that may be concatenated to form two 32-bit timers.

These timers can be used for general purpose timing when clocked from the system clock, or they can be connected to an external signal via a timer input pin. One timer is used to output a 25 MHz clock, on TOUT1, for the ethernet PHY. This clock is divided down from the MPC's system clock.

When connected to an external signal, the timers can count events or mark the occurrence of edges on those pins. One timer input, TIN3, connects to

the 1PPS signal to allow that timer to measure the 1PPS reference's timing relative to the internal system time.

Four independent baud-rate generators are provided for use by any of the internal serial ports. Each of these contains a 12-bit programmable counter (with optional ÷16 prescaler) to divide down either the internal CPU clock or an external clock to a suitable rate for a serial communications interface. The outputs of the four baud-rate generators can be independently routed to any combination of the serial controllers.

Interrupt Controller

The interrupt controller in the CPM combines and prioritizes interrupts from the CPM serial controllers, timers and DMA controller, before feeding them through to the main interrupt controller in the SIU (see "Interrupts" on page 43).

As well as the internal interrupt sources, the CPM interrupt controller can accept external interrupts through a number of input lines on parallel port C. In the ASIF these are used for sensing the power status lines (PWR_ON, PWD_EX, PWD_RX) from the reciter and the E lead from the E&M interface (see "E&M Interface" on page 79). This frees the software from having to regularly poll these input lines.

5.2.7 Communications Processor Interfaces

In the ASIF, the serial interface functions provided by the CPM are two UARTs, an I^2C port, an SPI port and a TDM PCM port.

The RISC processor in the CPM is supplemented by a serial communications controller (SCC), two serial management controllers (SMC), a serial peripheral interface (SPI) and inter-IC (I^2C) interface hardware. This hardware performs the lowest level operations such as bit shifting, clock recovery and FIFO buffering, to reduce the computation work load on the CPM RISC.

Serial Communications Controller (SCC)

Only one SCC, SCC1, is provided in the MPC859T. Consult chapters 21 through 28 of the MPC866 user's manual (reference 2) for a detailed description of the capabilities of the SCC.

An SCC can support a multitude of different serial formats, but in the ASIF, it is only used in UART mode for connection to the reciter internal UART port. Only the receive data, RISC_RS232_TXD[1], and transmit data, RISC_RS232_RXD1[1], lines are used to connect to the reciter. Although handshake inputs and outputs are available from SCC1, these are not used in the ASIF because the reciter does not support them.

1. This signal is named as per the reciter signal naming convention, hence the apparent contradiction in the signal name vs signal direction.

The data rate over this interface is transmitted at 115.2kbaud using standard asynchronous format with one start bit, eight data bits (transmitted lsb first), no parity, and one stop bit. Reception is similarly at 115.2kbaud; the receiver samples the received data at 16 times the baud rate to determine the approximate centre of the start bit, thus achieving bit synchronization. The 16x baud rate clock is generated internally by one of the four baud-rate generators.

To minimize software loading, the SCC incorporates 32byte FIFOs on both the transmit and receive paths, so that the software does not have to respond to the transmission or reception of each character. DMA is also available for facilitating data transfers from the SCC with minimal software overhead.

Serial Management Controllers (SMC)

The MPC contains two SMCs; SMC1 and SMC2. These are much less flexible than the SCC and can support only three modes of operation: UART, transparent mode and general-circuit interface mode. Consult chapter 29 of the MPC866 user's manual (reference 2) for a detailed description of these modes of operation.

SMC1 is used in UART mode and connects to the rear panel RS-232 serial port via an RS-232 transceiver (see "RS-232 Interface" on page 71). In UART mode the SMC does not provide any data FIFOs on the transmit or receive registers; only double buffering is provided. This requires that the data transfers from the SMC's registers be handled on a character by character basis by the CPM, rather than in larger blocks of characters. The SMC UART mode also does not provide any lines for hardware flow control ($\overline{\text{RTS}}$, $\overline{\text{CTS}}$). Hence, the software must provide any flow control through XON/OFF sequences.

The lack of FIFOs and hardware flow control require that the baud rate be limited, so that no data overflows occur with subsequent loss of characters. Typically, the baud rate that can be handled over an SMC UART channel is only $1/10^{th}$ of that possible with an SCC-implemented UART channel. The recommended maximum baud rate for the rear panel RS-232 port is therefore 115.2kbaud.

SMC2 is used in full-duplex, synchronous transparent mode. Whilst receiving, it simply captures a bit stream without any protocol or bit-level manipulation and transfers that bit stream data into memory. Transmission in transparent mode is similar, as no additional protocol overhead is added to the bit stream. Transparent mode requires a bit clock to sample the bit stream and transmit and receive synchronization signals to delimit the start of each character or word sent or received.

Compared to the SCC, transparent mode on the SMC provides less functionality, as it requires that bit clocks and synchronization signals be provided externally. SMC2 obtains these via the MPC's TDM interface (see "Time-Division Multiplexed (TDM) Port and Time Slot Assigner (TSA)" on page 57), which routes the bit clocks and word synchronization signals from the serial PCM stream produced by the reciter DSP.

Time-Division Multiplexed (TDM) Port and Time Slot Assigner (TSA)

Communication between the DSPs in the ASIF and reciter takes place over a PCM highway. This is a TDM bus supporting bi-directional full-duplex synchronous data transfers. The PCM highway contains six signals: transmit data, transmit frame sync., transmit clock, receive data, receive frame sync. and receive clock. These are also connected to the MPC's time slot assigner's (TSA) pins and DSP pins as shown in Table 5.8. The MPC has two TSA ports but only one is used in the ASIF.

Table 5.8 PCM Highway Connections

PCM Highway Signal	ASIF DSP Pins (I/O direction)	Reciter DSP Pins (I/O direction)	MPC Time Slot Assigner Pins
Transmit data	(O/P)	(O/P)	L1TxDA (O/P)
Transmit frame sync	(I/P)	(O/P)	L1TsyncA (I/P)
Transmit clock	(I/P)	(O/P)	L1TclkA (I/P)
Receive data	(I/P)	(I/P)	L1RxDA (I/P)
Receive frame sync	(I/P)	(O/P)	L1RsyncA (I/P)
Receive clock	(I/P)	(I/P)	L1ClkA (I/P)

Data transfers take place in periodic "frames", which are typically a multiple of the DSP software's sample rate. Within each frame, a number of "time slots" exist, each usually 8 or 16 clocks wide. The position of a time slot is determined relative to the frame sync signal, which signifies the start of a frame.

The serial data stream and synchronization signals for SMC2 are routed through the MPC's TSA. The TSA logic selects the data stream from a particular time slot, or combination of time slots, and routes it to the receiver data input of the SMC. Conversely, the TSA routes the transmit data output from the SMC and inserts the data stream into the selected time slot(s) in the frame. The transmit data outputs of the TSA and the DSPs are tri-stated when they are not active so that they can share the PCM highway.

Along with the data streams, the TSA routes the transmit and receive clocks to the SMC along with the transmit and receive sync signals. Transmitted bits are shifted out on the positive edge of the transmit clock and received bits sampled on the negative edge of the receive clock

Serial Peripheral Interface (SPI)

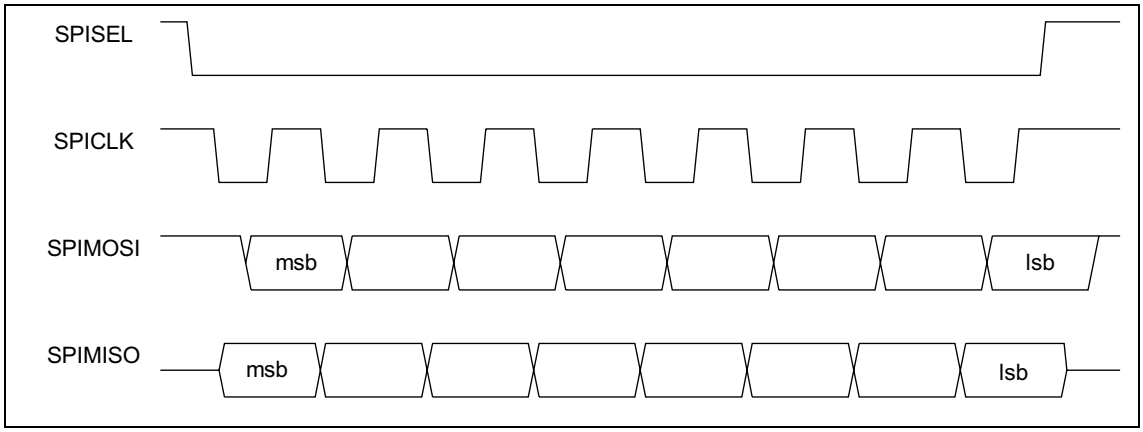
The SPI port is a simple full-duplex synchronous serial interface that connects to the SIO port on the reciter RISC. A data transfer between devices using SPI requires that one device be defined as the server and the other as a client device. The reciter RISC is the server device, so the MPC's SPI is configured as a client device. The MPC's SPI effectively emulates the SIO I/O expansion circuitry present on the analog SIF.

As the server, the RISC SIO generates a select signal ($\overline{\text{SPISEL}}$) to enable the MPC's SPI port for data transfer. The select signal enables multiple client devices to be connected to an SPI bus, but in the case of the reciter to ASIF connection, only one client, the MPC SPI port, exists. The reciter RISC SIO port also generates the shift clock (SPICLK); the data is shifted out on the negative-going edge of the clock and shifted in on the positive-going edge.

The clock shifts data in (on the SPIMISO pin) and out (on the SPIMOSI pin) of a single shift register, ie. as transmitted data is shifted out of the msb end of the shift register, received data is shifted in to the lsb of the same register. Since a single register is used for both receive and transmit data, it is necessary to read the received data before shifting in new data from the next transfer. The MPC's SPI port double buffers its SPI shift register to provide additional timing leeway for the software to recover the received data. The SIO port on the reciter RISC is not double buffered, so it is a limiting factor on the achievable transmission rate. The MPC's SPI port is capable of variable-length transfers, but the reciter RISC's SIO port is restricted to 8-bit transfers.

A typical set of waveforms is shown in Figure 5.6. Refer to chapter 30 of the MPC866 user's manual (reference 2) for a more detailed description of SPI operation.

Figure 5.6 SPI Transfer Waveforms



Inter-IC (I^2C) Bus

The I^2C bus is used to communicate with two peripheral devices: an E2PROM (U202) and the CODEC (U500). The E2PROM is used for storing configuration information related to the ASIF. The CODEC configuration is also performed via the I^2C bus (see "CODEC Digital Interfaces" on page 79). A more detailed description of I^2C bus operation may be found in reference 23.

The I^2C bus consists of two lines, SCL and SDA, which are driven by open-drain drivers and hence require the pull up resistors, R205 and R216. The MPC is assigned as the server device and drives the clock line, SCL. This clock determines the bit rate of the data transfers, which occur bi-directionally over the data line, SDA. The beginning and end of a message

is signified by a sequence of transitions on the SDA and SCL lines. I^2C data transfers must be in multiples of a byte.

Multiple devices can be connected to an I^2C bus, with each having a unique identifying address (see Table 8.1). The I^2C protocol incorporates an address byte (also including a read/write flag) at the beginning of each message so that the intended recipient can recognize it and respond appropriately.

Parallel Ports

Other lines from the CPM that are not otherwise used for serial interfaces, are used mainly as parallel inputs and outputs. These are detailed in Table 5.9; further description of their individual functions can be found in the referenced paragraphs.

Input signals on input port IPA[0..7] also connect to the PCMCIA interface input register (see "PCMCIA Interface" on page 44), so an interrupt can be generated on a change of state on those pins. Pins on port C can also be programmed to generate interrupts.

A hardware link, W201, is provided for enabling special modes for the ASIF. It is connected to a general-purpose digital input, PC9, and its function is determined in the software.

Table 5.9 Parallel I/O Ports

Pin Name	Direction	Function	Reference
PA0	O/P	Software test output 0	
PA1	O/P	Software test output 1	
PA2	O/P	Software test output 2	
PA3	I/P	1 PPS input/timer input	"Timers and Baud Rate Generators" on page 54 "1 PPS Input" on page 73
PA4	O/P	Status LED	
PA6	O/P	none	
PA10	O/P	none	
PA11	I/P	Ready sense	"Board Status Signal" on page 85
PA12	O/P	ASIF not ready	"Board Status Signal" on page 85
PA13	O/P	DSP reset	"Interrupts and Reset" on page 67
PB14	O/P	none	
PB15	O/P	Ethernet PHY power-down	"Ethernet PHY Configuration" on page 75

Table 5.9 Parallel I/O Ports (Continued)

Pin Name	Direction	Function	Reference
PB16	O/P	Reciter high-speed digital input 0	
PB17	O/P	Reciter high-speed digital input 1	
PB18	O/P	Reciter high-speed digital input 2	
PB19	O/P	Reciter Tx key	
PB20	O/P	Antenna relay control	"Antenna Relay Control" on page 73
PB21	O/P	M-lead output	"M-Lead Interface" on page 80
PB22	O/P	General-purpose digital output 6	"RSSI Output" on page 73
PB23	O/P	General-purpose digital output 7	"RSSI Output" on page 73
PC6	O/P	none	
PC7	O/P	none	
PC8	O/P	none	
PC9	O/P	Option link	
PC10	O/P	none	
PC11	O/P	none	
PC12	I/P	E-lead input	
PC13	I/P	Exciter power status	
PC14	I/P	Receiver power status	
PC15	I/P	Reciter power status	
IPA0	I/P	General purpose digital input 0	"General-purpose Digital Inputs" on page 72
IPA1	I/P	General purpose digital input 1	"General-purpose Digital Inputs" on page 72
IPA2	I/P	General purpose digital input 2	"General-purpose Digital Inputs" on page 72

Table 5.9 Parallel I/O Ports (Continued)

Pin Name	Direction	Function	Reference
IPA3	I/P	General purpose digital input 3	"General-purpose Digital Inputs" on page 72
IPA4	I/P	General purpose digital input 4	"Antenna Relay Control" on page 73
IPA5	I/P	General purpose digital input 5	
IPA6	I/P	Rx gate input	
IPA7	I/P	Co-ax relay input	
OP1	O/P none		
OP2	O/P	none	
OP3	O/P	none	

Parallel port pins that are not externally connected are set to outputs, so that the internally connected paralleled inputs do not float.

5.3 Memory

Two types of memory are connected to the MPC main bus: flash EPROM and synchronous DRAM (SDRAM). The flash EPROM is used mainly for storing the boot loader, a Linux kernel image and a compressed flash file system. The SDRAM is used as the main operating memory for storing both code and data.

5.3.1 Flash Memory

Flash EPROM (U301) is a standard 32Mbit (2Mx16) chip. The PCB footprint provides for an upgrade to a 64Mbit (4Mx16) chip for software expansion. Both types of chip have an internally segmented block structure, where each block can be individually erased or locked for protection. These chips also incorporate a unique identifier code and an OTP protection area, which can be used for product identification and software feature enabling. See the data sheet (reference 3) for details of the operation of this chip.

Code does not normally execute out of the flash EPROM, except during the boot load process: it is quite slow due to the need for performing two 16-bit memory fetches per 32-bit instruction for the MPC. The slow access time (70ns) of the flash also further slows execution speed, as five wait states have to be added to each memory cycle. The addition of wait states and other signal timing requirements are implemented by the GPCM (see "General-Purpose Chip Select Machine" on page 50).

5.3.2 Synchronous DRAM (SDRAM)

The main memory for executable code and data is normally provided by two 256Mbit SDRAM chips (U300 and U302), each 4M x 16 bits x 4 banks. Together, these provide 64Mbytes (16Meg of 32-bit words) of memory.

The SDRAM PCB footprints also provide for expansion to 512Mbit parts, each 8M x 16bits x 4 banks, giving a total of 128Mbytes of memory; or a decrease to 64Mbit parts, each 1M x 16bits x 4 banks, giving 16Mbytes total. Configuration changes for different size SDRAM chips is mainly accommodated through reprogramming the UPM (see "User-Programmable Machines" on page 51). The exception is for the 64Mbit parts, which require a hardware change as shown in Table 5.10.

Table 5.10 SDRAM Hardware Configuration

SDRAM Size (Mbits)	R301	R302
64	not fitted	33R
128	33R	not fitted
256	33R	not fitted
512	33R	not fitted

Reference should be made to the data sheet (reference 4) for details of the SDRAM chips. A full description of the operation of SDRAMs is outside the scope of this document; the application notes (references 5 and 6) should be referred to for a more detailed explanation.

SDRAM Control Inputs

The x16 SDRAM chips are paired to provide a 32-bit data bus to match the MPC's data bus width. The MPC always reads and writes 32-bit words, but individual bytes can be written by using the byte select lines, $\overline{BS}[0..3]$. These byte selects are connected to the appropriate byte mask inputs (DQML and DQMU) of the SDRAMs; when these inputs are high they prevent data being written into the corresponding byte of the memory location.

Other control lines, row address strobe ($\overline{RAS}$), column address strobe ($\overline{CAS}$), write enable ($\overline{WE}$) and chip select ($\overline{CS}$), control the mode of operation of the SDRAM. All the control signals are synchronously timed using the clock input (CLK): signals are latched on the rising edge of CLK.

An exception is the clock enable signal, CKE; if this is taken low the SDRAM goes into a low-power standby mode and ignores all other inputs, including the CLK signal. This mode is not used in the ASIF and hence CKE is permanently tied high.

The CLK signal is generated by the MPC. For EMC reduction the clock line is series terminated by resistor R204. An AC-coupled shunt termination, R303 and C317, cleans up residual reflections on the clock line.

Address Multiplexing and Command Codes

Like other DRAM types, SDRAMs use multiplexed address inputs (A0 - A11) to reduce the number of package pins. Initially the row addresses (usually the higher order addresses) are latched from the address inputs, then the column addresses (lower order addresses) are latched. The row addresses are latched into the SDRAM by the row address strobe, $\overline{RAS}$, while the column address are latched by the column address strobe, $\overline{CAS}$.
The multiplexing of the address lines is performed within the MPC under the control of UPMA (see "User-Programmable Machines" on page 51). The UPM also generates the row address strobe and column address strobe at the appropriate times.

Unlike other DRAM types, SDRAMs also use the multiplexed address lines, in conjunction with the control lines, to enter command codes (Table 5.11) and SDRAM mode settings.

Table 5.11 SDRAM Command Codes

Code	Function	Control and Address Inputs					
		A0-A11	A10	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
ACT	Bank activate	V	V	L	L	H	H
BST	Burst stop	X	X	L	H	H	L
DESL	Device deselect	X	X	H	X	X	X
MRS	Mode register set	V	V	L	L	L	L
NOP	No operation	X	X	L	H	H	H
PALL	Precharge all banks	X	H	L	L	H	L
PRE	Precharge selected bank	V	L	L	L	H	L
READ	Read access to one bank	V	L	L	H	L	H
READA	Read access with auto-precharge	V	H	L	H	L	H
REF	Auto-refresh	X	X	L	L	L	H
WRITE	Write access to one bank	V	L	L	H	L	L
WRITEA	Write access with auto-precharge	V	H	L	H	L	L

V = valid address, L= low, H = high, X = don't care

SDRAM Initialisation

After power up, the SDRAM chips must be initialized and set to their correct operating mode before being used. Prior to setting the operating mode, the internal nodes in the SDRAM must be stabilized to their normal working voltages. After a time delay of 200us from power up, a precharge all banks command is executed to set up the internal nodes for subsequent memory cycles. Then, at least 8 refresh cycles (see "SDRAM Refresh Cycles" on page 64) must be executed. Finally, the mode register set command is issued to set the following parameters:

- burst length = 4 (see "SDRAM Burst Cycles" on page 64)
- burst write enabled
- sequential address mode
- $\overline{\text{CAS}}$ latency = 2

After a short time delay, the SDRAM is ready for normal operation.

SDRAM Read and Write Cycles

The sequence of events for a single memory location write cycle is as follows:

- Set up row address and ACT command
- Set $\overline{\text{WE}}$ line inactive (high), $\overline{\text{OE}}$ line to active (low)
- Strobe in address and command with $\overline{\text{RAS}}$ going low
- Set up column address and WRITE command
- Strobe in address and command with $\overline{\text{CAS}}$ going low
- Wait 2 clock cycles ($\overline{\text{CAS}}$ latency)
- Latch data
- Raise $\overline{\text{CAS}}$
- Set up PRE command
- Raise $\overline{\text{RAS}}$
- Ready for next cycle

SDRAM Burst Cycles

The MPC memory interface achieves high memory bandwidth by utilizing the burst feature of SDRAMs. This allows multiple, adjacent address locations to be read or written without inputting new addresses each time, thus saving considerable time per access. During a burst access, an SDRAM can read or write new data every clock cycle after the initial memory access.

The SDRAM burst size is set to four words to match the MPC RISC CPU internal cache line refill size (see "Memory Caches and Memory Managers" on page 40). Allowing for the setup time for the initial memory access, a burst of four words can be fetched from memory in only 8 memory clock cycles. With a memory clock of 62.5MHz, the SDRAMs can deliver sufficient instruction code to the MPC for it to execute in excess of 30MIPs, even when performing a cache refill.

SDRAM Refresh Cycles

All dynamic memory devices use memory cells that indicate the state of a bit by the level of charge stored on a minuscule capacitor. This charge can leak away over a period of time so it is necessary to periodically top it up. This is accomplished by executing a refresh cycle on each row in the memory array. For the SDRAMs every row must be refreshed at least once every 64ms.

Although all rows could be refreshed in one block every 64ms, to do so would prevent the MPC from accessing its memory for an extended period. It is preferable to perform refreshes on a distributed basis, ie. one row every

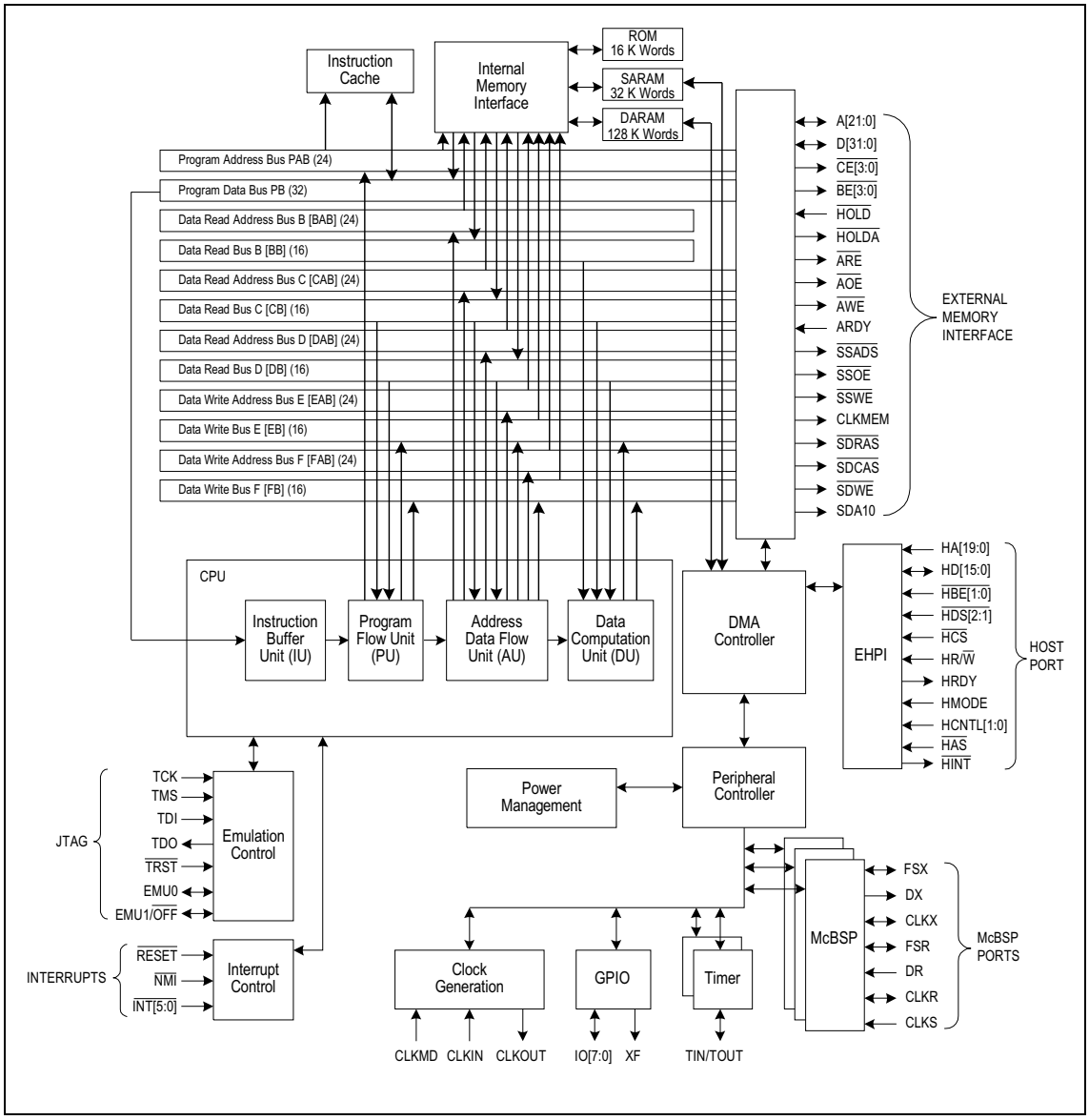
8us, to minimize the disruption to MPC memory accesses. The issuing of refresh cycles is handled automatically by the UPM (see "User-Programmable Machines" on page 51) using its periodic timer to determine the refresh interval.

5.4 DSP

5.4.1 DSP

A TMS320VC5510 digital signal processor chip is provided for the vocoder and other signal processing functions. It is a high-performance 16-bit fixed-point DSP capable of operating at up to 160 MIPs. Refer to the TMS320VC5510 data sheet (reference 7) and functional overview (reference 8) for details of the DSP characteristics. Figure 5.7 shows the internal architecture of the DSP.

Figure 5.7 DSP Block Diagram



Processor Core

The TMS320VC5510 DSP has a 16-bit core with extensive instruction pipelining for high performance. See the CPU architecture description (reference 9) for details. Internally, the DSP utilizes a Harvard architecture with separate sets of address and data buses for program code and data accesses. The program address bus is 24 bits wide while the program data bus is 32 bits wide. Multiple internal data buses, each 16 bits wide, and address buses, each 24 bits wide, enable simultaneous data fetches or writes to multiple memory blocks (see "Internal Memory" on page 68).

Where a program code fetch or data access cannot be satisfied from the internal memory space, it is routed to external memory through the external memory interface (EMIF) controller. For external accesses, both program and data accesses occur over a unified 32 bit data bus and 22 bit address bus, ie. a von Neumann type architecture.

The DSP incorporates a multi-channel DMA controller to facilitate rapid data movement without requirement intervention from the DSP core. This DMA controller can transfer data between the internal memory, external memory and peripherals. It is also used as part of the host port interface (see "Host Port Interface (HPI)" on page 69 for details). The operation of the DMA controller is described in reference 10.

To facilitate program development, the DSP provides debugger access to its internals through a modified JTAG test port brought out on connector J106. This connector is not fitted to production boards. A full description of the JTAG interface is outside the scope of this document; reference 22 should be consulted for details.

Interrupts and Reset

The DSP provides for six external interrupt inputs, although only one is used for the ASIF. An external 1 PPS timing reference (see "1 PPS Input" on page 73) is connected to $\overline{\text{IRQ0}}$, the highest priority maskable interrupt input. This is used for providing the DSP with a server timing reference, should it be required in simulcast networks. All other interrupt inputs are tied to their inactive high state.

Interrupt facilities are also available between the DSP and MPC. The DSP program can interrupt the MPC using the $\overline{\text{HINT}}$ output. The MPC can also interrupt the DSP using an internal interrupt register in the host port interface (see "Host Port Interface (HPI)" on page 69).

The MPC controls the DSP reset line via a parallel output port (PA13) so that it can force the DSP into reset to halt a runaway program, or to restart the boot load process (see "Boot Loading" on page 68). If the MPC is reset, output PA13 goes tri-state and resistor R200 pulls the $\overline{\text{DSP\_RST}}$ line low, thus also resetting the DSP.

Peripherals

Aside from the McBSP ports (see "Serial Interfaces" on page 71), the DSP provides a limited set of peripherals: an 8-bit parallel I/O port, a single bit output flag and two timer/counters. See the DSP peripheral reference guide (reference 11) for details.

None of these peripherals are used in the ASIF application, but some of the parallel port lines and the output flag are brought out to test points for software debugging purposes. Three of the parallel I/O ports share pins with the boot mode selection pins (see "Boot Loading" on page 68), but, after reset is released, these can also be used as standard parallel I/O.

Clock Generation

To achieve high performance, the DSP requires high frequency clock. To minimize EMC generation this high-frequency clock is generated internally to the DSP chip by multiplying up a relatively low-frequency reference clock input using an internal phase-locked loop (PLL). The input reference clock (CLKIN) can be multiplied by various ratios ranging from 0.25 to 31 with the proviso that the final PLL operating frequency must lie in the range 80 MHz to 160 MHz.

The actual multiplication ratio is set by programming an internal PLL register; in the ASIF this will typically be set to 12, giving a DSP clock of 153.600MHz from the 12.800MHz reciter reference clock. An exact (subject to reference clock tolerances) 2.048MHz CODEC clock may be readily derived from this 153.6MHz clock with a divide-by-75 counter.

Optionally (see "Clock Oscillator" on page 81), the DSP reference clock may be changed to the on-board 13.000MHz crystal oscillator. Multiplying this reference clock by 11.5 gives a DSP clock of 149.500MHz. Dividing this clock by 73 gives an approximate 2.048MHz (-27ppm error) CODEC clock; this is sufficiently accurate for many applications.

Prior to the program being able to set up the PLL register, the DSP operates in a PLL bypass mode where the DSP is operated directly from the reference clock, or half the reference clock. This is determined by the CLKMD input, which is tied low to select the 1:1 mode. Once the DSP program is up and running, it programs the PLL registers, enables the PLL, and switches to operating from the internal high-frequency clock.

Internal Memory

No external memory is provided for the DSP, so all code and data has to be stored in the on-chip memory. This consists of 160k of 16-bit half-words made up of eight blocks, totalling 32k words, of dual-access RAM (DARAM) and 32 blocks, totalling 128k half-words, of single-access RAM (SARAM). Each type of internal memory can be accessed in a single clock cycle, ie. zero wait states.

With DARAM, the DSP core can make two accesses (reads, writes or both) to a single block of memory during a single clock cycle. DARAM enables more efficient implementation of many DSP algorithms such as filtering, buffering, etc. SARAM is limited to a single access (read or write) during a clock cycle. Typically, SARAM is used for storing program code and coefficient tables.

Since no external memory is used, most of the pins relating to the memory interface (A[21..0], D31..0] et al.) are left unconnected. The exceptions are the ready signal (ARDY) and bus hold ($\overline{\text{HOLD}}$); these are tied to their inactive high states so that the DSP software does not hang indefinitely if it erroneously attempts to access an external memory location. To prevent excessive current drain caused by the data bus pins floating, these are held at valid logic levels by internal "bus keeper" circuits. The current drain can also be reduced by shutting down the EMIF circuitry.

Boot Loading

As the DSP has no external program memory from which to start program execution, it must start up in a boot loader mode to get program code from an external source into its internal memory. The DSP incorporates a small block (16k half-words) of ROM containing a boot loader program. See reference 12 for details of the boot loader program operation.

By default, the DSP starts executing from the boot loader ROM when its reset is released. One of the first operations of this boot loader program is to

read the state of the boot mode selection pins to determine the required boot load source. Four boot mode selection pins, BOOTM[3..0], specify the mode in accordance with Table 5.12.

Table 5.12 DSP Boot Mode Selection

BOOTM[3..0]	Boot Mode
0000	No boot
0001	Serial SPI E2PROM boot from McBSP0 (24-bit addressing)
0010 - 0111	Reserved
1000	No boot
1001	Serial SPI E2PROM boot from McBSP0 (16-bit addressing)
1010	Parallel EMIF boot from 8-bit asynchronous memory
1011	Parallel EMIF boot from 16-bit asynchronous memory
1100	Parallel EMIF boot from 32-bit asynchronous memory
1101	HPI boot
1110	Standard serial boot from McBSP0, 16-bit element length
1111	Standard serial boot from McBSP0, 8-bit element length

In the ASIF, the boot mode pins are strapped through resistor network R402 to select HPI boot mode. In this mode the boot loader does not load any code but merely jumps to a fixed location (0x10000) in its memory and executes the pre-loaded code found there.

It is the responsibility of the MPC to pre-load the DSP program code via the HPI (see "Host Port Interface (HPI)" on page 69). While the MPC is loading this code, the DSP must not be allowed to start executing this code. To accomplish this, the DSP incorporates a bit in an HPI control register, which is cleared by a power-on reset. While this bit is clear the DSP does not execute its application code. When the MPC has completed loading the DSP code, it sets this bit in the HPI control register, signaling the DSP to jump to the start location and execute the loaded program.

5.4.2 Host Port Interface (HPI)

The DSP is connected to the MPC using the Host Port Interface (HPI): this makes the DSP's internal memory space accessible as a memory mapped peripheral in the MPC's address space. Through the HPI, the MPC has access to the bottom 1Megaword of the DSP memory space except for the DSP's peripheral and control registers. Hence, the MPC accessible memory includes all of the DARAM and SARAM, plus a portion of the external DSP memory, if fitted.

The HPI has two modes of operation: multiplexed and non-multiplexed address/data; the ASIF uses non-multiplexed mode as selected by the HMODE pin. In non-multiplexed mode, the host port appears to be a single large window into the DSP memory space. Actually, only two 16-bit registers exist in the DSP, the data register HPID and the control register HPIC; the transfer of data to and from the DSP memory takes place under control of the internal DMA controller. This gives the appearance, to the host processor, of the entire DSP memory space being accessible, albeit with some delay due to the need for the DMA controller to gain access to the internal memory.

For a write operation to the HPI, the MPC places the desired address on the host port address bus, HA[0..19], and data to be written on the host port data bus, HD[0..15]. The HCNTL line, connected to address line A20, is set high to indicate an access to the data register. The host port chip select ($\overline{\text{HCS}}$), read/write (HR_W) and write data strobes ($\overline{\text{HDS2}}$) are activated as appropriate. This latches the data into the HPID register, which acts as a temporary holding register. From there, the DMA controller in the DSP transfers the data to the correct location in DSP memory, as determined by the address on HA[0..19].

A read operation from the HPI follows the same sequence, except that the MPC must wait until the data is fetched from the DSP memory, by the DMA controller, before the MPC memory cycle can be completed. The MPC memory controller inserts wait states until the DSP indicates that the memory cycle can be completed by taking its HRDY output high.

This is connected through to the MPC's $\overline{\text{TA}}$ input (see "MPC Bus Cycles" on page 48), via flip-flop U204 and tri-state buffer U212, to terminate the bus cycle. U212 is controlled by flip-flop U204 to ensure the $\overline{\text{TA}}$ timing is synchronized to the MPC's memory clock. When the DSP is not selected, it outputs its HRDY signal as high, ie. a false HRDY signal. To prevent this false HRDY signal prematurely terminating a DSP access cycle or other non-DSP bus cycles, flip-flop U204 is inhibited from clocking, by gate U213, when the DSP chip select, $\overline{\text{HCS}}$, is inactive.

Shortly after the DSP chip select, $\overline{\text{CS2}}$, is asserted, it continues to output a false HRDY signal until its internal logic recognizes the $\overline{\text{HCS}}$ input and outputs the correct HRDY state. To prevent this delayed HRDY response generating a $\overline{\text{TA}}$, prematurely terminating the bus cycle, gate U213 continues to inhibit flip-flop U204 from clocking for approximately 150ns after $\overline{\text{HCS}}$ has been asserted. The delay is provided by RC network R223 and C210, while diode D201 and resistor R225 ensure that the delay circuit quickly recovers in time for the next cycle. A direct, undelayed path through the other input of U213 ensures the flip-flop U204 is reset, and $\overline{\text{TA}}$ negated, immediately after $\overline{\text{HCS}}$ has been negated.

Note U204, U212 and U213 are omitted from current network boards. The MPC performs a wait following each write cycle to DSP memory.

5.4.3 Serial Interfaces

Two separate Multi-channel Buffered Serial Ports (McBSP) are used to communicate with the ASIF CODEC chip (McBSP0) and the reciter DSP (McBSP1). A third McBSP channel (McBSP2) is available, but is not used in the ASIF design. These ports implement a high-speed synchronous serial interface with bi-directional data transfer. The transmit and receive operations on these ports may operate independently, but, in most applications, they are operated at the same data and sample rates. Reference 14 should be consulted for details of the operation of these McBSP ports.

McBSP0 connects to the CODEC (see "CODEC Digital Interfaces" on page 79) and is used for transferring audio data to and from that chip at the audio sample rate, ie. 8.0kHz. The CODEC data is formatted as 15-bit linear PCM code, but is transmitted, msb first, on port DX0 using a 16-bit frame for ease of handling within the DSP. Data is simultaneously received on port DR0, enabling full-duplex operation. The bit rate is 2.048 MHz and the frame sync rate is 8.0KHz, ie. the sample rate.

As the CODEC chip is a client device, McBSP0 is configured as a server device, ie. it generates the clocks and sync signals for the CODEC. The CODEC does not require separate transmit and receive clocks, so a clock output is generated on the transmit clock output, CLKX0, and fed back to McMSP receive clock input, CLKR0, as well as the CODEC clock input, PCMCLK. To synchronize the data frames within the bit stream, the DSP outputs a transmit frame sync signal, FSX0, which is fed back to the McBSP receive sync input, FSR0, as well as the CODEC sync input, PCMSYNC.

McBSP1 is used to transfer data to and from the reciter DSP. The interconnections are detailed in Table 5.8. The receive port lines (DR1, FSR1, CLKR1) are configured as inputs, as the reciter DSP generates all the relevant clock and sync signals. On the transmit side, the McBSP outputs all the signals (CLKX1, FSX1, DX1) for reception by the reciter DSP. The bit rate is 12.8 Mbps. The frame sync line is active high for one bit following a 16-bit data transfer.

5.5 I/O Buffers

5.5.1 RS-232 Interface

A basic RS-232 interface, supporting only the RxD and TxD lines, is provided on the ASIF for connection to external serial devices such as dispatchers, terminals and PCs. The interface is configured as DCE mode and connection is made through a rear panel DB9 socket, which is pin-out compatible with IBM PC serial cables.

The RS-232 level signals, RS232_TXD and RS232_RXD, are converted to LVTTL levels using dual RS-232 transceiver U600 (ADM3202). This device incorporates an internal charge pump to generate the positive and negative supply voltages required for RS-232 compatibility. Clamping diodes D603 and D604 protect against excessive voltages for short periods; prolonged application of voltages in excess of ±15V may blow fuse F601 or resistor R620. EMC filtering components are provided on both RS-232 lines.

5.5.2 General-purpose Digital Inputs

Four general-purpose digital inputs, DIG0_IN through DIG3_IN, are also provided for external status signals, or configuration and mode setting. These are also connected through the DB9 connector, with their pin allocations being such that they do not conflict with the operation of the RS-232 interface. The description below covers only one input circuit, as the others are identical

Considering input DIG0_IN, the input signal passes through EMC filtering components E602 and C605, before passing through a noise filter, R637 and C649. This filter, with a nominal time constant of 270us, provides some degree of noise rejection, but this is generally not sufficient to debounce switch or relay contact inputs, which require further software debouncing. The filtered output passes through inverting Schmitt trigger U602, which squares up the signal and converts it to the LVTTL levels required by the MPC. U602 has LVTTL compatible input threshold levels, but can withstand input voltages to +5.5V.

A switch, or relay contact to ground, may be used on the input as a suitable pull-up resistor (R603), is provided on board. This pull-up resistor is sourced from a +5V supply and supplies approximately 1mA to the switch or relay contact. Generally, switches or relays with gold-plated contacts are recommended for reliable operation with this relatively low current and voltage.

Alternatively, the input can be directly connected to the outputs of most logic families running from 3.3V supplies or above. The exceptions are low voltage (<5V) CMOS logic that does not have 5V compatible outputs and 4000 series CMOS logic running from 5V or lower supplies, which does not have enough drive capability to sink the pull-up current. In such cases, the input pull-up resistor should be removed from circuit.

The input is protected for momentary application of ESD voltages or surge voltages of up to ±50V, but prolonged application of excessive voltage may fuse the pull-up resistor R630 or series resistor R637. The input voltage to U602 is clamped by diode array D605 to ground or the +5V supply. In the event that the input voltage is forced above +5V, excess current will flow through resistor R630 and diode D605; Zener diode D610 diverts this excess current to ground, maintaining the efficacy of the protection clamp.

5.5.3 1 PPS Input

The 1 PPS input circuitry is similar to that for the general-purpose digital inputs, except that the filter (R641 and C653) time constant is considerably reduced to approximately 500ns. Having a much lower nominal time delay preserves the required timing accuracy of the 1 PPS edges, despite component tolerance variations, etc.

The incoming 1 PPS signal is normally supplied via a 50Ω coaxial cable from a distribution amplifier outputting a 5Vpp level. To ensure that there are no reflections, which might cause jitter on the leading edge of the timing pulse, this cable is AC terminated with network R600 and C609. AC termination is used to maximize the peak signal level; the full 5Vpp level is available as against the 2.5Vpp that would be available with DC termination.

5.5.4 Antenna Relay Control

A single high-current output driver is provided for general-purpose use, although its normal usage is for controlling an antenna switchover relay. It has an open collector output and can sink currents of up to 250mA from supply voltages up to 30V. Instead of controlling a relay, it is also suitable for driving sounders, LEDs, and small incandescent lamps. With incandescent lamps, their size should be limited such that the initial turn-on current does not exceed 250mA, to avoid overstressing the output transistor.

The relay driver is controlled by parallel output port PB20 of the MPC. The current drive from this port is boosted by pre-driver transistor Q601, which, in turn, drives the output transistor, Q600. Q600 is protected from voltage spikes from inductive loads by Zener diode D602. Excess current protection is provided by fuse F600. The output can also be used for driving logic inputs that are TTL compatible, as resistor R636 pulls the output up to +5V when Q600 is turned off.

Should the output function not be required, the driver transistor can be turned off permanently and the line used for an extra input, DIG4_IN. An input circuit similar to that used for the other digital inputs is paralleled with the output circuit.

Note The antenna relay feature is not supported in all software versions.

5.5.5 RSSI Output

The reciter generates a differential analog RSSI signal strength indication output. This differential output is converted to single-ended, amplified and buffered by U601 on the ASIF. Ignoring transistors Q603a and Q603b, resistors R651, R657, R658 and R660-R663 set the gain of op-amp U601 to amplify the difference between RSSI+ and RSSI- by approximately 1.64. They also compensate for the 2.4V standing bias levels on the RSSI+ and RSSI- lines. The output of U601 is protected by resistors R601 and R631,

and Zener diode D601, before passing through the customary EMC filtering components.

Op amp U601 is powered from the +5V supply, so it only supports a 0V to 5V output range, as opposed to the 0V to 6.5V range for the standard analog SIF board. This restriction is for compatibility with logic devices connected to the RSSI output. Should the analog output function not be required, the RSSI output can be used as a general-purpose logic level output. Transistors Q603a and Q603b are controlled by parallel output lines PB22 and PB23 from the MPC and can be used to force the output high or low respectively. Any high-speed logic device connected to this output should use Schmitt trigger inputs to avoid oscillation, due to the relatively slow transition time of U601's output.

Note The RSSI output feature is not supported in all software versions.

5.6 Ethernet Interface

5.6.1 Ethernet Physical Interface

The FEC in the PowerQUICC does not incorporate the physical level interface hardware for direct connection to an ethernet network, so an ethernet PHY is required. This function is provided by U700, a 10/100Mbps ethernet transceiver with twisted pair interface. This device, and the FEC, are both capable of operating at either 10Mbps or 100Mbps, half or full duplex, and may use auto negotiation.

The incoming signals on the ethernet receive twisted pair are coupled through isolation transformer T700b and passed to the differential receive data inputs, RXP and RXN, of U700. The line is terminated by resistors R705 and R706, while excess voltage spikes are clamped to supply, or ground, via diode array D700.

Differential outgoing signals, TXP and TXN, from U700 are also transformer isolated through T700a before being transmitted to line. Line termination is provided by R710 and R711, with overvoltage clamping performed by D700. Common mode termination of the transmit and receive pairs is provided by R712 and R713. Unused pairs in the ethernet cable are terminated by R715 and R716 and connected to chassis ground through C723, to minimize noise coupling to the active pairs.

U700 provides several LED driver outputs, LED0 through LED3, for indicating the status of the PHY. LED0 output indicates whether the U700 is connected to a network and whether data reception or transmission is taking place: flashing indicates reception or transmission, whilst steady indicates a link has been established. LED3 output indicates whether a collision has occurred during transmission.

The internal logic of U700 runs from a +2.5V supply, which is generated from the +3.3V supply by an internal voltage regulator. Its output, VCC25OUT, is fed back to power the internal logic, as well as supplying the line transformers.

5.6.2 Ethernet PHY Configuration

The PHY is configurable for various operating modes and speeds, by software control of internal mode register settings, or by sensing the state of various pins on power up.

Software configuration of the internal registers in PHY is accomplished over the Serial Management Interface (SMI) from the MAC. Data is transferred on a bi-directional data line (MDIO) and latched on the rising edge of the clock (MDC) supplied from the MAC. Refer to the AC101L data sheet (reference 17) for a listing of the configuration registers.

As an alternative to SMI configuration, some of the PHY register settings can be made through strapping external pins; the state of these pins is sensed on the rising edge of RST and latched into the internal registers. These mode setting pins have internal pullups, so will read high if left unconnected.

Table 5.13 PHY Configuration Settings

Pin	Reset State	Mode Selection
LED0/Burnin#	High	Burnin disabled
LED1/SPD100	High	100Mbps enabled
LED2/Duplex	High	Full duplex enabled
LED3/ANEN	Low	Auto-negotiate mode disabled
CRS/Repeater	Low	Repeater mode disabled

Since the MDIO line is bi-directional, the PHY status can also be read back via the SMI. Refer to the AC101L data sheet (reference 17) for a listing of the status registers. To indicate a change of status the PHY can output an interrupt request on its $\overline{\text{INTR}}$ pin; this goes to a general-purpose interrupt input, $\overline{\text{IRQ4}}$, on the MPC.

One further hardware pin, $\overline{\text{PDOWN}}$, is used to put the PHY into a low-power standby mode when taken low. This pin is driven by a general-purpose output, PB15, from the MPC.

5.6.3 Ethernet PHY Clocking

Timing of the internal operations of the ethernet PHY requires an external 25.000MHz clock source. This is provided from a timer output, TOUT1, of the MPC to the XI input of the PHY. The timer divides down from the MPC clock, hence this must be an exact multiple of 25MHz. Internal to the PHY, the 25MHz clock is multiplied by a PLL to 125MHz, to form the line symbol bit rate clock: 100Mbps ethernet encodes the line data, so that 5 bits are transmitted for every 4 input bits, hence the line bit rate is 125MHz.

The PHY outputs a 25MHz clock (for 100Mbps) or 2.5MHz (for 10Mbps) on the TXCLK for timing the data transfers over the MII (see "Media Independent Interface (MII)" on page 76). For received data, the PHY regenerates a clock from the incoming data stream and divides this by four to output a 25MHz or 2.5MHz clock on the RXCLK output.

5.6.4 Media Independent Interface (MII)

The PHY connects to the MPC FEC via a Media Independent Interface (MII). This is an 18 line bus (including the SMI lines) for connecting multiple PHYs to a MAC, although in the ASIF's case, only one PHY is used. Data transfer to/from the FEC occurs over separate receive and transmit buses, each four bits wide, and are clocked by RXCLK and TXCLK respectively, supplied from the PHY.

On reception of a valid signal on the receive line inputs, the carrier sense (CRS) line goes active. Shortly after, Receive Data Valid (RXDV) goes high, indicating the presence of valid data on the MII receive data bus, RXD[3..0]. Data on this bus is latched into the FEC on the rising edge of the RXCLK clock. Should an error be detected in the received signal, the Receive Error (RXER) line goes high; this is also latched on the rising edge of RXCLK.

On transmission, the FEC places data on the transmit data bus, TXD[3..0], and asserts TXEN high, to indicate valid data on the bus. The data is latched into the PHY on the rising edge of TXCLK and is then formatted for transmission to line via the transmit data outputs. If, for any reason, the FEC needs to abort a transmission, it asserts the transmit error (TXER) line; this causes the PHY to transmit an invalid signal, which will be detected by the remote receiver.

With ethernet, there is a potential for two devices to transmit to the network simultaneously, causing a data collision. While a transmission is in progress, the receiver section monitors the network for a collision condition. Should one occur, the Collision (COL) output is set high, indicating to the FEC that it has to retry the transmission later.

5.7 Audio and E&M Interface

The audio and E&M interface provides a basic four-wire (4W) analog audio and a DC signalling path into the base station for interconnection with existing analog infrastructure. It is designed to be compliant with telco requirements for 4W leased circuits, so that it can be directly connected to telco cable networks. It is not suitable for connection to the PSTN.

5.7.1 CODEC

A single channel CODEC chip, U500, performs the conversion to/from the PCM signals from the DSP to the analog interface signals. Internally, this device supports an independent receive channel and an independent transmit channel, which together provide a 4W audio interface capable of full-duplex operation. Both the receive and transmit channels have internal switching which allows them to be routed to one of two sets of external pins on the device, but this switching function is not used on the ASIF. Refer to the CODEC data sheet (reference 15) for details on the internal architecture.

Note The CODEC data sheet defines the transmit and receive channels with respect to the PCM interface direction. Hence, data transmitted to the DSP is derived from an input signal from the analog interface. Data received from the DSP is processed by the CODEC to become an analog output. The description below uses the same direction convention.

CODEC Transmit Operation

Considering first the transmit direction, an incoming signal on the balanced lines RA and RB passes through EMC filtering components, E507, E508 and C516, and is coupled through capacitor C512 to line transformer T501. On the secondary side of T501, the incoming signal is divided down with resistive divider R508, R505 and R509 to match the input level requirements of the CODEC microphone inputs, MIC1P and MIC1N. The signal input to the CODEC is internally amplified, converted to digital, filtered and sent to the DSP over the PCM interface. The other microphone inputs, MIC2P and MIC2N, are not used and are shorted together through C504.

The combined total of R505, R508 and R509 provides the correct transformer loading to present a 600Ω load to the line input. Capacitors C508 and C510 compensate for the leakage inductances in the transformer to optimize the input return loss at the upper end of the audio band.

CODEC Receive Operation

In the receive direction the digital data received from the DSP is digitally attenuated and filtered, converted to analog and then applied to an output routing switch. This switch routes the output signal to an output power amplifier, and subsequently to balanced outputs, EAR1OP and EAR1ON. The unbalanced output, EAR2O, is not used in the ASIF design.

The CODEC power supply rail of 3.3V limits the maximum output swing on each of the EAR1OP and EAR1ON outputs to approximately 2.3Vpp. Since this is not sufficient, if connected directly through a line transformer, to provide the required output levels to line, an additional amplifier stage, comprising dual op-amp U501 and its associated components, is added.

This differential input, differential output amplifier circuit boosts the CODEC differential outputs by approximately 2dB, as determined by resistors R521, R522, R530, R531, R533 and R535. As this is greater than the required gain, the input signal is attenuated approximately 3.7dB by resistors R502, R520, R516 and R517. Filter capacitor C520 removes any residual high frequency noise on the CODEC outputs.

The two op-amp differential outputs connect to the line transformer T500 via sense resistors R532 and R534. The correct transformer drive resistance is synthesized by taking positive feedback, through R533 and R535, and negative feedback, through R530 and R531, from these sense resistors. With the resistor values shown, the differential output resistance of the amplifier is approximately 402Ω, the value for optimum return loss. Capacitors C507 and C509 optimize the high-frequency return loss as for the transmit side.

The synthesized output resistance enables a greater output swing from a given power supply voltage than is possible using a real output resistor; the amplifier is capable of driving in excess of +6dBm to a 600Ω line over the 300-3400Hz voice band. Due to limitations in the line transformer's signal handling capability at low frequencies, the allowable output level has to be progressively reduced to a maximum of -14dBm at 67Hz. Higher output levels at low frequencies result in excessive, mainly third harmonic, distortion.

When connected to a telco line, the output level must be limited to the maximum of 0dBm at all frequencies for compliance with the telco regulations. Due to CODEC gain inaccuracies and external circuit variations totalling ±1.5dB, the nominal maximum output level is downgraded to -1.5dBm to ensure that the maximum allowable line level is not exceeded.

Since the telco network can present large transient voltages to equipment, two levels of overvoltage clamping are provided in the audio line interface. Initially, transients are absorbed by bi-directional transient suppressors D504 and D503. Any residual transient signals that are coupled through the transformers are further clamped to the supply and ground rails by diode array D505 on the transmit channel and by Zener diodes D506 and D507 on the receive channel.

The level of protection provided by the transient suppressors and clamping diodes is regarded as "secondary" protection only: if extreme conditions are expected, "primary" overvoltage protection devices, such as arrestors, may need to be fitted externally.

5.7.2 CODEC Digital Interfaces

The CODEC supports two different types of digital interface: an I^2C interface for configuration setting and a PCM-type interface for transferring the digital audio data.

Codec Configuration Interface

The I^2C interface connects to the MPC and is used to set internal control registers for operating mode, signal routing, gain settings, power control and tone generation. The transfer of data is similar to an I^2C access to the E2PROM (see "Inter-IC (I2C) Bus" on page 58) except that CODEC occupies a different address in the I^2C address range (see "Appendix A – I2C Device Addresses" on page 103). Refer to the CODEC data sheet (reference 15) for full details of the internal control registers.

Codec Data Interface

The PCM interface of the CODEC is connected to the McBSP port 0 of the DSP using a subset of the McBSP signal lines. Data, in 15-bit linear coded PCM format, is transferred out of the CODEC on the PCMO output and into the CODEC on the PCMI input. Data bits are shifted out of PCMO, msb first, on the positive-going edge of the PCMCLK clock signal and shifted into PCMI on the negative-going edge.

The PCMCLK clock is provided from the McBSP port transmit clock, CLKX0; since this is a steady 2.048 MHz, it is also used for the server clock input (MCLK) to the CODEC for its internal timing. To synchronize the bit streams the CODEC also requires a frame synchronization signal, PCMSYNC, which is supplied from the McBSP transmit sync signal, FSX0, which pulses at the nominal sample rate of 8KHz.

5.7.3 E&M Interface

An E&M (ear and mouth) signalling interface is provided, along with the audio interface, to implement signalling function that is compatible with basic telephony signalling circuits. This consists of an output circuit, the M-lead, and an input circuit, the E-lead. Typically, M-lead function would be assigned as an RX-GATE output and the E-lead as the TX-KEY input to the base station.

Normally, in telephone switching circuits, the M-lead would switch to ground and the E-lead would be connected to the -48V exchange battery to sense the current flow into the battery. Basic E&M signalling can then be implemented by connecting the M-lead of one device to the E-lead of another device, and vice versa.

Actually, for the ASIF, two leads are brought out for each interface to provide fully floating switch and sensor circuits. This facilitates the connection of the E&M interface to signalling circuits other than standard telephony E&M interfaces. This flexibility comes at a price, as the voltage source for the E-lead must now be wired externally to the ASIF. Any voltage source from 5 to 50V is suitable, but it will have to be suitably isolated from

the base station supplies if the isolation voltage requirements for the audio interface are to be maintained.

M-Lead Interface

The M-lead is used for outgoing signalling and is controlled by an opto-MOS relay DS500a; this device has a pair of MOSFETs connected to form a switch and is driven by a photovoltaic diode illuminated by an LED. When on, the switch is capable of conducting in either direction. The input LED is driven by emitter follower Q501a. This emitter follower boosts the output current drive of the MPC output pin, PB21.

Overvoltage protection for the switch is provided by D501, which is followed by the usual EMC filtering. Protection device D501 has an SCR type structure so it latches on in response to a transient. In the event that a low resistance DC source is connected to the M-lead, a prolonged excess current could eventually damage the EMC inductors or the PCB tracking. Fuse F501, in series with the M-lead, protects against this eventuality.

E-Lead Interface

When E-lead current flows through the input LED of opto-isolator DS500b, it causes the opto-transistor to conduct pulling input PC12 of the MPC low. This input is also paralleled with an interrupt input, IRQ6, for rapid software response from the MPC.

As the E-lead can be sourced from a wide range of voltages, it is necessary to have some form of current limiter in series with the opto-coupler, so that its maximum current rating of 50mA is not exceeded. A bi-directional current limiter circuit comprising transistors Q500, Q503 and Q504 accomplishes this, limiting the maximum current to approximately 6mA. Back-to-back LEDs are used in DS500b so that the E-lead interface responds to current flow in either direction.

Considering first the Ea lead being positive with respect to the Eb lead, transistor Q503 is turned on by base resistors R512 and R513. Current flows through one LED of DS500b, diode D500a, transistor Q503 and resistor R514 before returning through the Eb lead. When the current flow is such that the voltage drop across R514 reaches approximately 600mV, NPN transistor Q504a starts conducting and diverts base current from Q503. With less base current, Q503 progressively comes out of saturation, limits the current flow, and acts as a current limit.

Operation with the Ea and Eb lead polarities reversed is identical, except that current flows through Q500 and D500b with PNP transistor Q504b acting to control the current flow.

The E-lead incorporates protection and EMC filtering as for the M-lead.

5.8 Clock Oscillator

Both the MPC and DSP incorporate phase-locked loops to generate their respective high frequency clocks from a relatively low reference frequency. On the ASIF, separate reference frequencies can be used for the MPC and DSP: the MPC reference is supplied from an on-board 13MHz oscillator, while the DSP reference is supplied from either the 13MHz oscillator or the reciter 12.8MHz clock. The reciter 12.8MHz clock is normally used, so that the DSP is operated in frequency synchronization with other reciter clocks.

The 13.000MHz VCTXCO, Y200, provides a clipped sinewave output of approximately 1Vpp, which is amplified and buffered by inverter U800 to produce an LVTTL clock signal. This is fed to the reference clock input of the MPC, RISC_CLK, via damping resistor R806 to minimize overshoot and reflections, and preserve signal quality on the MPC clock input.

To ensure that clipped sinewave is amplified symmetrically, preserving the duty cycle, the output of the VCTCXO is capacitively coupled into the input of buffer U800. This device is then biased into the centre of its linear region via its feedback resistor, R808.

When the reciter 12.8MHz clock is used as the DSP PLL's reference, the clock signal, DSP_CLK_IN, from the reciter is buffered by U801.This is then passed to the DSP reference clock input, DSP_ CLK, via damping resistor R806.

For other applications, where the ASIF may not be attached to a reciter, the internal 13.000MHz clock may be routed to the DSP reference clock. In this case, resistor R806 is omitted and resistor R805 installed.

5.9 Power Supply

The MPC and DSP require dual supply voltages, +1.8V and +1.6V respectively, for their core logic and +3.3V in each case for their I/O drivers. Most of the other devices on the board use +3.3V, except for the analog output and the general-purpose inputs, which use +6V supplies.
The maximum operating current drains are 370mA from the +3.3V supply, 180mA from the 1.8V supply, 120mA from the 1.6V supply and 12mA from the +6V supply. To minimize heat dissipation, all supplies are generated from the incoming +28V supply using switching regulators.

The +3.3V and +1.8V supplies are generated by a dual-phase buck switching converter, U900; this device incorporates two switch-mode controllers, which are operated on opposite phases of a common clock. This arrangement forces the input current pulses from the two switchers to add out of phase, thus reducing the peak ripple current drawn from the input supply. The lower ripple current injects less noise back into the input supply, hence input filtering requirements are less onerous.

5.9.1 +3.3V Switching Regulator

Firstly, consider the +3.3V switching regulator on the RHS of U900. This is a conventional buck regulator with a synchronous rectifier to maximize switching efficiency with low output voltages. MOSFET Q901a is switched at a suitable duty cycle (approximately 3.3/28), to chop the input voltage to produce the required average output voltage of 3.3V. Since Q901a is an n-channel MOSFET, its gate must be pulled several volts above the input supply to ensure it is fully saturated when switched on. An external boost voltage circuit, C915 and D900, produces a gate supply, on pin BST2, that swings at least 5V above the main supply rail. The internal gate driver for the upper MOSFET is powered from this pin.

The synchronous rectifier, MOSFET Q901b, maintains current flow through the inductor when the upper MOSFET is switched off. Since the MOSFET has a lower voltage drop than the paralleled diode, D905, efficiency is improved when it is switched on. Diode D905 carries the inductor current only during the short transition period, switching between the upper and lower MOSFETs.

The chopped waveform from the MOSFETs is filtered by L901 and C918 to produce a smooth DC output. The output voltage is fed back through resistive divider R909 and R910 to close the control loop. These resistors are proportioned to provide 0.8V, the internal reference voltage, when the output voltage is 3.3V. Since U900 uses a current-mode control strategy, the sensed output voltage does not directly control the switcher duty cycle, but, instead, controls the average inductor current required to maintain the specified output voltage. The inductor current is sensed by differentially monitoring the voltage drop across R908.

Following the main filter, there is another filter, E902 and C929, to remove residual high frequency noise. Bulk output capacitor C972 provides/sinks current for short periods, until the control loop of the switching regulator can restore normal regulation, to cover any sudden load changes.
The control loop of the regulator is stabilized by the loop compensation components, C916, R906 and C926, which connect to the output of the internal error amplifier.

5.9.2 +1.8V Switching Regulator

The 1.8V switcher on the LHS of U900 is identical to the 3.3V switcher, except for changes to resistor values, to set the output voltage (R900 and R901) and the current sense (R902). Because of the large step-down ratio (28V/1.8V), the on time of the upper MOSFET, Q900a, is quite short. To meet the minimum on time requirements of the switch-mode controller, its operating frequency has to be set to its minimum, nominally 250KHz. This is accomplished by grounding the PLL filter pin; U900 has an internal PLL to synchronize its operating frequency to an external source, but this mode of operation is not used in this design.

5.9.3 +1.6V Switching Regulator

The +1.6V DSP core supply is sub-regulated from the +3.3V supply with another switching regulator, U910. This device is also a current mode controller and operates in a similar fashion to U900. It differs in that the output MOSFETs and current sense resistor are contained internally for reduced PCB area. Its higher operating frequency of 1.5MHz allows the use of a much smaller smoothing inductor, L910. An output filter, E910 and C949, and bulk capacitor C973, are provided, as for the +3.3V and +1.8V outputs.

5.9.4 Auxiliary Supply

An auxiliary supply is used to power some of the switching regulator internal circuitry, as well as providing the input to the +6V regulator (see "+6V Regulator" on page 84). Some of the operating current for the U900 is derived from the auxiliary supply, through its EXTVcc supply pin.

With no voltage, or a low voltage, on EXTVcc, the power requirements for the internal circuitry of U900 are derived from the main +28V supply using an internal 7.5V(nominal) linear regulator. This normally occurs during the initial power supply startup phase. When the voltage on EXTVcc exceeds approximately 7.3V, an internal power switch disconnects the linear regulator from the internal supply rail, INTVcc, and the U900 internal circuitry draws its current directly from the auxiliary supply. Since the internal linear regulator no longer wastes power dropping the +28V input down to 7.5V, the overall power supply efficiency is increased, providing that the auxiliary supply is generated by a suitably efficient method.

The auxiliary supply is derived from the main +3V3 switcher using a charge pump voltage tripler circuit, comprising Q902, Q903, C921, C922, C930 and D909-D911. The operation of this circuit can be explained by considering the voltage waveforms across the series combination of the filtering inductor L901 and sense resistor R908. When the switching regulator has reached a steady state, the voltage at the junction of R908 and C918 will be approximately constant at +3.3V, whereas the junction of L901 and D905 will be switched between 0V and 28V by the action of chopper transistors Q901a and Q901b.

With Q901b conducting, capacitor C922 will charge from the +3.3V output via diodes D909a and D910b. Capacitor C921 will charge in a similar fashion through diodes D909b and D910a. When Q901a turns on (and Q901b turns off), the junction of L901 and D905 will be pulled up to +28V, reverse biasing D910a and D910b. Zener diode D908 will also be reverse biased; when it breaks down, MOSFETs Q903 and Q902 will turn on. Diodes D909a and D909b are also reverse biased during this process.

Note In this circuit, n-channel MOSFETs Q902 and Q903 are operated in the reverse conduction mode, ie. positive current flow is from source to drain. The MOSFETs are operated in this mode because, in normal connection, the inherent substrate diode

would conduct, and prevent the charge pump capacitors fully charging.

With both Q902 and Q903 conducting, capacitors C921 and C922 are connected in series and stacked on top of the +3.3V supply. The voltage on the stacked capacitors is peak rectified by diode D911 and reservoir capacitor C930. With ideal diodes and MOSFETs, the peak rectified voltage would be 9.9V, ie. three times the +3V3 supply. In practice, the diode voltage drops and MOSFET conduction losses reduce the attainable voltage to approximately 8.0V.

5.9.5 +6V Regulator

A +6V supply is used for some of the audio and I/O buffer circuitry. This has a relatively low current drain, so it is linearly regulated from the auxiliary supply using U602. For lower supply, noise capacitor C970 filters the regulator's internal reference voltage, and output capacitor C923 provides additional smoothing on the output, to minimize noise coupling into the audio circuitry.

5.9.6 Power Sequencing and Start-up

Both the +3.3V and +1.8V switching regulators incorporate soft-start circuits to minimize the inrush current surge and hence minimize stresses on the power components. During start-up, the output of the error amplifier is also clamped by the soft-start circuit so that the allowable inductor current rises slowly, minimizing the inrush current to the power supply. The rise time is controlled by a constant current charging the soft-start capacitors C913 and C911.

The soft-start circuits also play a role in the fault protection circuitry of U900. If an over-current condition is detected, the soft-start capacitors are progressively discharged, lowering the inductor peak current limit. Should the capacitors discharge sufficiently, the switching regulators will shut down completely and require that the input power be cycled before they will start up again. This behavior may be undesirable, eg. during circuit debugging; two resistors, R912 and R913 (each 2M21), may be optionally fitted to disable this latching shut-down function.

With devices such as the MPC and DSP using dual supply voltages, it is imperative that the correct sequencing of these voltages be maintained during power-up and power-down. This is enforced by clamping diodes D901, D902, D906 and D907. These prevent the +1.8V or +1.6V supplies exceeding the +3.3V rail by more than a diode drop. They also limit the maximum differences between the +3.3V supply and +1.6V and +1.8V supplies to approximately 2.4V and 1.8V, respectively.

5.9.7 Power-on Reset

A power-on-reset signal is required for initializing various chips on the board; this is provided by CPU supervisor chip U901. On power up this chip asserts its $\overline{\text{RST}}$ output low and holds it low until the +3.3V supply reaches its normal operating voltage. U901 also incorporates a further time delay of 240ms (nominal) to allow other circuitry to stabilize before releasing $\overline{\text{RST}}$.

Since U901 monitors only the +3.3V supply, use is made of the Power-Good (PGOOD) status signal from U900 to ensure that the +1.8V supply is also within specification before releasing RST. PGOOD is an open-drain output that pulls low if either the +3.3V or +1.8V supplies deviate from their nominal value by more than 7.5%. When PGOOD goes low it reduces, through R911 and R907, the supply voltage seen by U901, thus forcing a reset condition. Switch S900 also simulates a power supply voltage drop to U901, allowing a manual reset operation.

Neither the +1.6V nor the +6V supplies are monitored by the power-on reset circuit.

5.9.8 Board Status Signal

Since the ASIF and reciter digital board have separate power converters, it is inevitable that one board powers up before the other. If the powered board drives signal lines to the unpowered board, there is a potential for damage to occur, through chip latch-up, when the second board powers up.

In order to coordinate the power-up sequence between the ASIF and the reciter digital board a hardware handshaking line, ASIF_RDY, is provided. This is controlled by the power-on reset circuit and the MPC to indicate the ASIF's readiness to run: when the ASIF is not ready to run it holds the ASIF_RDY line low. By sensing the level on this line, the reciter board can determine whether the ASIF is powered up and ready to run. However, the current reciter hardware design does not support the ability to sense this line.

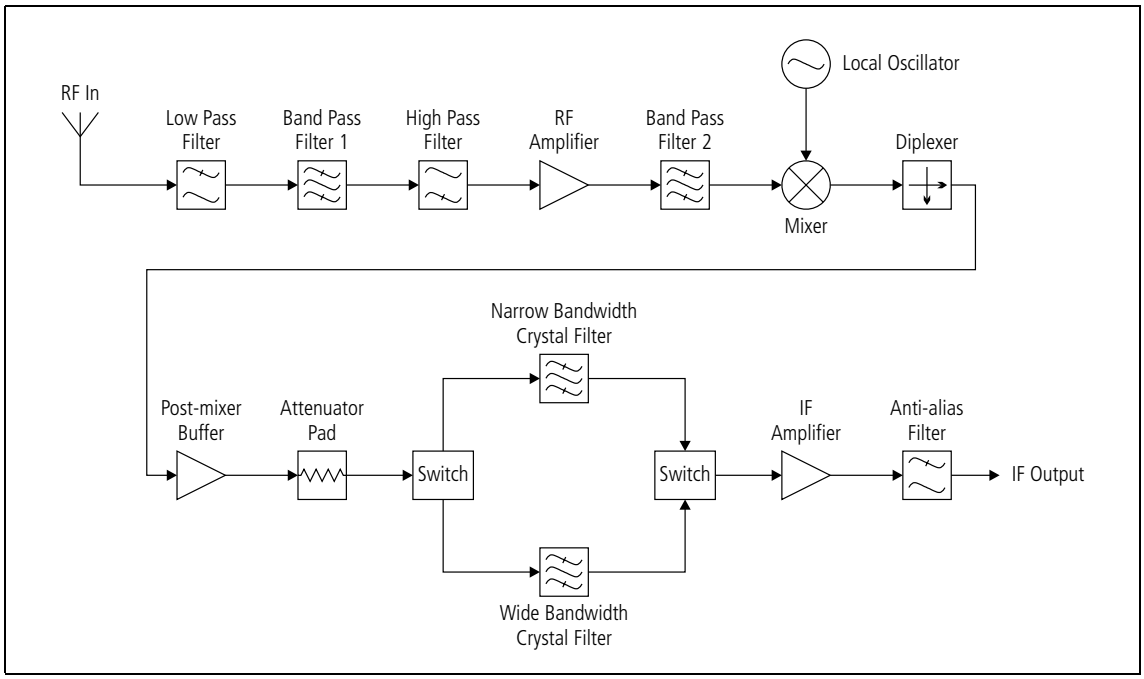
When the ASIF is not powered, the ASIF_RDY line is held low through D903a. When the ASIF is powered-up, but still held in reset, the ASIF_RDY line is held low through D903b. When the power-on reset is released, ASIF_RDY remains held low by transistor Q910. Finally, when the ASIF MPC has completed its initialization, it drives the ASIF_NRDY line low, turning off Q910. The ASIF_RDY line is then pulled high by R922, indicating that the ASIF is ready to run.

The ASIF_RDY handshaking line can also be used by the ASIF to determine the status of the reciter digital board. As yet, no hardware has been implemented on the reciter board to fully support the function of the handshake line, so the ASIF is limited to sensing the status of the reciter's main supply voltage. A +3.3V supply line is available from the reciter on pin 7 of connector J101: if this supply is not present, the ASIF_RDY line is pulled low through diode D100.

6 RF Circuitry

6.1 Receiver RF Circuitry - VHF Reciter

Figure 6.1 Reciter VHF Receiver RF Circuitry Block Diagram



6.1.1 Front End

The incoming signal from the BNC connector is fed through a low pass filter, then through a band pass "doublet" filter, and finally through a high pass filter. These networks attenuate harmonics and spurious responses. The signal is then amplified and passed through another band pass "doublet" filter before being passed to the mixer.

6.1.2 Mixer

The RF signal from the front end is converted down to the 16.9 MHz IF by a high level (+17 dBm local oscillator) mixer. The voltage controlled oscillator (VCO) generates a level of 20 dBm which is fed to the mixer through an attenuator pad. A diplexer terminates the IF port of the mixer in 50Ω, thus ensuring a good match for all mixing products, as well as enhancing the linearity. The post-mixer buffer amplifier provides gain and isolation between the mixer and crystal filter. It also compensates for the insertion loss of the crystal filter.

6.1.3 IF Circuitry

The signal from the mixer is fed to the IF amplifier through a 2-pole crystal filter which provides protection from strong off-channel signals. Note that there are two 2-pole crystal filters, one for narrow bandwidth and one for wide bandwidth. The appropriate filter is selected by software-controlled PIN switches, according to the bandwidth selected in the CSS.

The IF amplifier is a two-transistor design with voltage and current feedback, which provides sufficient gain to drive the digital receiver. The 16.9MHz signal is finally passed to the analog-to-digital converter (ADC) in the digital receiver via an anti-alias filter. This filter prevents IF noise at frequencies above 16.9MHz, generated in the amplifier, from being sampled by the ADC at other Nyquist zones.

6.1.4 Synthesizer

The receiver synthesizer consists of a programmable frequency synthesizer IC, the receiver VCO, and a stable known reference.

The synthesizer uses a phase-locked loop to lock the receiver VCO to a stable known frequency reference. The synthesizer IC receives the divider and control information from the RISC processor via a 3-wire serial bus (clock, data and enable). When the data bits are latched in, the synthesizer processes the incoming signals from the VCO feedback signal (f_{vcofb}) and the reference oscillator (f_{ref}).

The VCO feedback attenuator is a resistive divider that terminates the VCO feedback signal in a fixed low impedance (50Ω). This attenuates the VCO RF level down to a level suitable for the RF prescaler (within the synthesizer IC).

A 12.8MHz temperature controlled crystal oscillator (TCXO) is used as the internal reference oscillator. When the TCXO is active, the receiver synthesizer is locked to an "internal reference mode" (by default). Alternatively, a phase-locked 12.8MHz voltage controlled crystal oscillator (VCXO) can be used as the external reference oscillator. When the VCXO is active, the receiver synthesizer is locked to an "external reference mode". In operation only one oscillator is active at any given time. Refer to "Reference Switch" on page 29 for details on the phase-locked 12.8MHz external reference oscillator.

The reference oscillators are buffered, branched, and divided down to the 3.125kHz (default) or 2.5kHz divider reference within the synthesizer IC. The same divider reference is maintained by dividing the VCO feedback signal using the prescaler and programmable dividers of the synthesizer IC. Phase lock is achieved when both divider references have the same phase and frequency content (i.e. their difference is zero or DC). This is achieved by the phase detector (part of the synthesizer IC), which compares both divider references and delivers an error signal. A ±4mA charge pump circuit (also part of the synthesizer IC) and the active loop filter circuit convert this error

signal to a DC voltage (0 to 22V[1]) to tune the VCO for correction. The loop filter has a bandwidth of 150Hz and filters the VCO control lines, reference side bands and spurious signals.

Note The VCO frequency increases as the control line voltage increases.

6.1.5 VCO

The receiver VCO consists of a high Q VCO, low noise amplifier, harmonic filter, fixed slope attenuator, and a final driver. Refer to Figure 6.2 on page 90.

High Q VCO

The VCO BJT transistor operates in a common emitter, Colpitts oscillator configuration (virtual ground at the base). The LC resonator is coupled between the collector and base. A high Q trimmer is coupled to the base end, and varactor diodes are coupled to the collector end. This forms a high Q resonator which is both mechanically and electronically tunable. Mechanical tuning is possible by adjusting the trimmer. Changes in the control voltage from the loop filter are applied to the varactors to facilitate electronic tuning.

Low Noise Amplifier

A BJT cascode amplifier is used as a broad band isolator and low noise amplifier. This has internal self-bias circuitry, and the output provides enough RF power to drive the following stages.

Harmonic Filter

The VCO has a relatively high harmonic content. A third order low pass elliptic filter is used to attenuate this content.

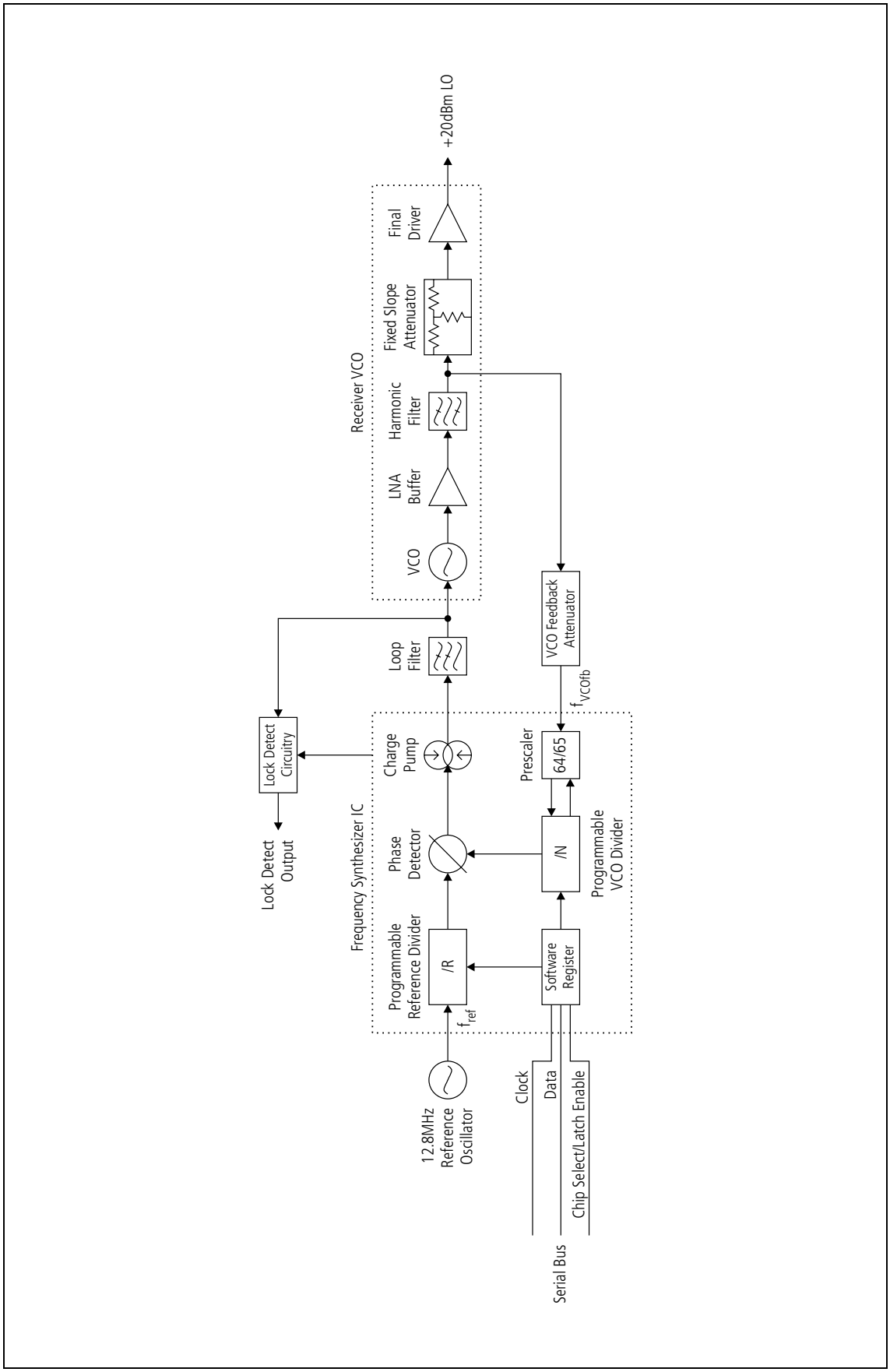
Fixed Slope Attenuator and Final Driver

A silicon BJT is used as a broad band matched Class A final driver to drive the +20dBm local oscillator port of the mixer. To maintain a fixed output level, a fixed slope attenuator is introduced at the input to the final driver so that the attenuation rate (slope) increases with an increase in frequency.

The B band VCO frequency spans from either 152.9MHz to 164.9MHz, or 164.9MHz to 190.9MHz, according to the product type. The VCO is tuned to 16.9MHz above (high side injection) to produce the 16.9MHz IF signal at the output of the mixer.

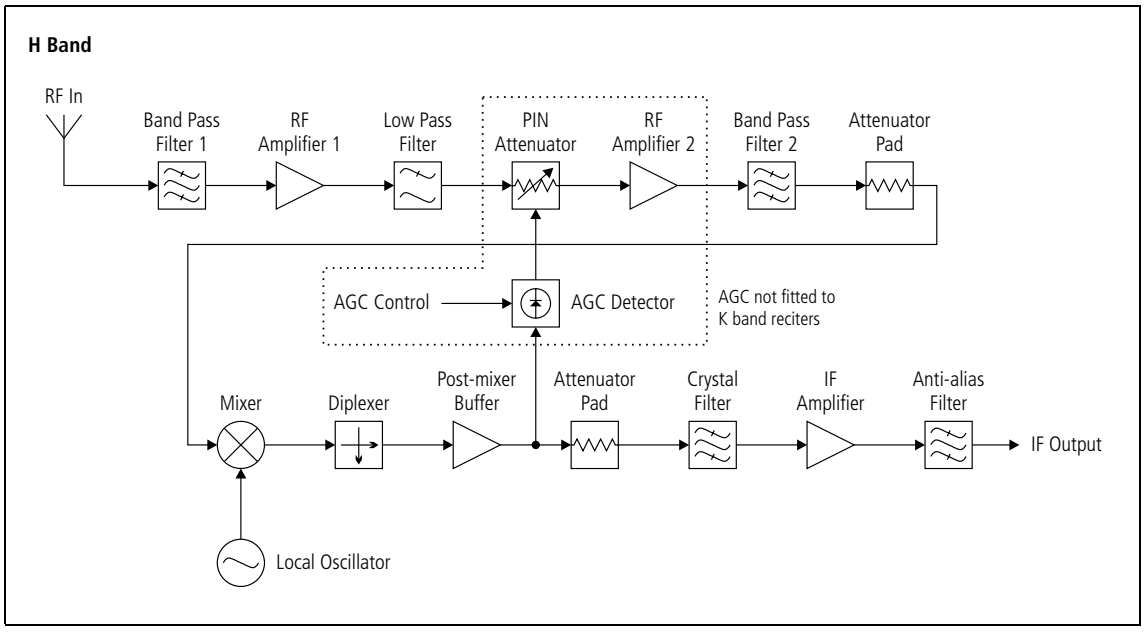
1. The normal lock range is between 3V and 16V.

Figure 6.2 Reciter Receiver Synthesizer Block Diagram



6.2 Receiver RF Circuitry - UHF Reciter

Figure 6.3 Reciter UHF Receiver RF Circuitry Block Diagram



6.2.1 Front End

H Band Reciter

The incoming signal from the BNC connector is fed through a triplet helical filter, followed by a simple low pass network which attenuates harmonics and spurious responses from the preceding filter. The signal is then amplified and passed through a low pass filter which provides immunity to interference from higher frequency out-of-band signals. Automatic gain control (AGC) is provided at this point by a PIN diode attenuator. The signal is now amplified again in a second RF amplifier, and is then fed through a band pass filter and attenuator pad to the mixer.

6.2.2 Mixer

The RF signal from the front end is converted down to the 70.1 MHz IF by a high level (+17 dBm local oscillator) mixer. The voltage controlled oscillator (VCO) generates a level of 20 dBM which is fed to the mixer through an attenuator pad. A diplexer terminates the IF port of the mixer in 50Ω, thus ensuring a good match for all mixing products, as well as enhancing the linearity. The post-mixer buffer amplifier compensates for the insertion loss of the crystal filter, and any excess gain is reduced by the following attenuator pad.

6.2.3 IF Circuitry

The signal from the mixer is fed to the IF amplifier through a 4-pole crystal filter which provides protection from strong off-channel signals. The IF amplifier is a two-transistor design with voltage and current feedback, which provides sufficient gain to drive the digital receiver. The 70.1MHz signal is finally passed to the analog-to-digital converter (ADC) in the digital receiver via an anti-alias filter. This filter prevents IF noise at frequencies other than 70.1MHz, generated in the amplifier, from being sampled by the ADC at other Nyquist zones.

6.2.4 Synthesizer

The receiver synthesizer consists of a programmable frequency synthesizer IC, the receiver VCO, and a stable known reference.

The synthesizer uses a phase-locked loop to lock the receiver VCO to a stable known frequency reference. The synthesizer IC receives the divider and control information from the RISC processor via a 3-wire serial bus (clock, data and enable). When the data bits are latched in, the synthesizer processes the incoming signals from the VCO feedback signal (f_{vcofb}) and the reference oscillator (f_{ref}).

The VCO feedback attenuator is a resistive divider that terminates the VCO feedback signal in a fixed low impedance (50Ω). This attenuates the VCO RF level down to a level suitable for the RF prescaler (within the synthesizer IC).

A 12.8MHz temperature controlled crystal oscillator (TCXO) is used as the internal reference oscillator. When the TCXO is active, the receiver synthesizer is locked to an "internal reference mode" (by default). Alternatively, a phase-locked 12.8MHz voltage controlled crystal oscillator (VCXO) can be used as the external reference oscillator. When the VCXO is active, the receiver synthesizer is locked to an "external reference mode". In operation only one oscillator is active at any given time. Refer to "Reference Switch" on page 29 for details on the phase-locked 12.8MHz external reference oscillator.

The reference oscillators are buffered, branched, and divided down to the 6.25kHz (default) or 5kHz divider reference within the synthesizer IC. The same divider reference is maintained by dividing the VCO feedback signal using the prescaler and programmable dividers of the synthesizer IC. Phase lock is achieved when both divider references have the same phase and frequency content (i.e. their difference is zero or DC). This is achieved by the phase detector (part of the synthesizer IC), which compares both divider references and delivers an error signal. A ±4mA charge pump circuit (also part of the synthesizer IC) and the active loop filter circuit convert this error signal to a DC voltage (0 to 22V[1]) to tune the VCO for correction.

1. The normal lock range is between 3V and 16V.

The loop filter has a bandwidth of 150 Hz and filters the VCO control lines, reference side bands and spurious signals.

Note The VCO frequency increases as the control line voltage increases.

6.2.5 VCO

The receiver VCO consists of a high Q VCO, low noise amplifier, harmonic filter, fixed slope attenuator, and a final driver. Refer to Figure 6.2 on page 90.

High Q VCO

The VCO BJT transistor operates in a common collector, Colpitts oscillator configuration, and uses a shorted quarter-wave ceramic coaxial resonator. The open end of the resonator is terminated by a combination of a high Q trimmer and varactor diodes. This forms a high Q resonator which is both mechanically and electronically tunable. Mechanical tuning is possible by adjusting the trimmer. Changes in the control voltage from the loop filter are applied to the varactors to facilitate electronic tuning.

Low Noise Amplifier

An N-channel dual gate MOSFET is used as a broad band matched Class A low noise amplifier. It has internal self-bias circuitry, and the output provides enough RF power to drive the following stages.

Harmonic Filter

The VCO has a high second harmonic content. A third order low pass elliptic filter is used to attenuate this content.

Fixed Slope Attenuator and Final Driver

A silicon-based BJT transistor is used as a broad band matched Class A final driver to drive the +20 dBm local oscillator port of the mixer. To maintain a fixed input level, a fixed slope attenuator is introduced at the input to the final driver so that the attenuation rate (slope) decreases with an increase in frequency.

The H band VCO frequency spans from either 369.9 MHz to 409.9 MHz, 399.9 MHz to 449.9 MHz, or 470.1 MHz or 510.1 MHz, according to the product type. The VCO is tuned to either 70.1 MHz below (low side injection) or above (high side injection) to produce the 70.1 MHz IF signal at the output of the mixer.

6.2.6 AGC (H Band Only)

The AGC is used to prevent the ADC from being overloaded by strong interfering signals present at the receiver antenna port. The AGC loop consists of a PIN diode attenuator, AGC buffer, and detector. The pick-off point for the AGC is the output of the post-mixer buffer. The input signal to the AGC is buffered, amplified and then detected. The detected DC voltage is buffered and fed to PIN_CTRL to control the attenuation of the PIN attenuator.

To prevent overload of the ADC, the peak level at its input should not exceed 0 dBm. This corresponds to –30 dBm at the antenna connector, and approximately –22 dBm at the AGC pick-off point. The AGC operates over a range of approximately 11 dB.

The AGC circuit can be enabled or disabled using the CSS.

6.3 Exciter RF Circuitry

Refer to Figure 6.4 on page 95 and Figure 6.5 on page 97.

6.3.1 Frequency Control Loop

Audio modulation of the exciter synthesizer is implemented in the frequency control loop (FCL). It uses a three-point modulation scheme involving the FCL_VCXO and VCO signals.

The FCL consists of reference oscillators, clock buffers, twisted ring counter phase detectors, low pass filters (LPFs), ADCs, the FCL processor and digital-to-analog converters (DACs).

Reference Oscillators

Modulation to the FCL_VCXO reference oscillator requires the use of the FCL_VCXO_CTRL and SYN_VCO_MOD signals to apply:

- a constant DC offset to the FCL_VCXO signal until it achieves frequency lock to the internal referenced TCXO;
- frequency modulation to the FCL_VCXO and VCO simultaneously from the transmit audio signal; the transmit audio signal has a range of 0 to 3 kHz.

The modulated signal from the VCXO is attenuated by the bandwidth of the loop filter in the low pass filter (i.e. 150 Hz). To obtain flat modulation across the audio band, the VCO is also modulated simultaneously to obtain a composite high pass filter response. Figure 6.4 shows the relationships between the frequency modulation gain characteristics of the VCXO and VCO.

Clock Buffers

The TCXO and VCXO signals are squared up and buffered as digital signals using hex inverters.

Twisted Ring Counter

The VCXO and TCXO signals are phase shifted and multiplied by XOR (exclusive_or) logic. This is achieved using a twisted ring counter, which also divides both signals by four.

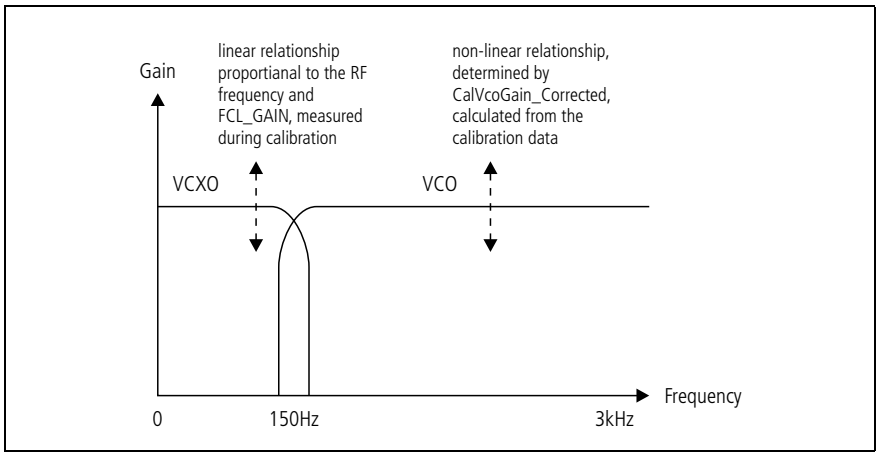
Low Pass Filter

There are two output signals from the twisted ring counter. Both signals have the sum and difference frequency contents of the TCXO and VCXO signals, but there is a 90° phase difference between them.

I and Q low pass filters capture the difference frequency contents down to DC and integrate them to form two triangular waves, which are 90° out of phase with each other. This frequency is equal to a quarter of the difference frequency content of the TCXO and VCXO signals.

The in-phase triangle frequency is referred to as "I channel" and the quadrature-phase triangle frequency is referred to as "Q channel".

Figure 6.4 Comparison of VCXO and VCO Modulation Responses



ADC

The I_Q channel triangular analog waveforms are sampled and transformed to digits using a 16-bit ADC with a signal-to-noise ratio of 75 dB.

FCL Processor and DAC

The FCL processor runs a DSP-based algorithm which takes the digitized signals, I_Q and transmit audio, and compares them to the transmit modulation calibration data.

Using the compared results it attempts to lock FCL_VCXO to the TCXO, as well as modulate the FCL_VCXO and VCO signals to achieve modulation flatness across the transmit audio and VCO RF bands.

The FCL processor achieves this by sending the digitized modulation code through a16-bit DAC. Here the code is translated to analog signals which modulate FCL_VCXO and the VCO. The DAC has a signal-to-noise ratio of 70 dB.

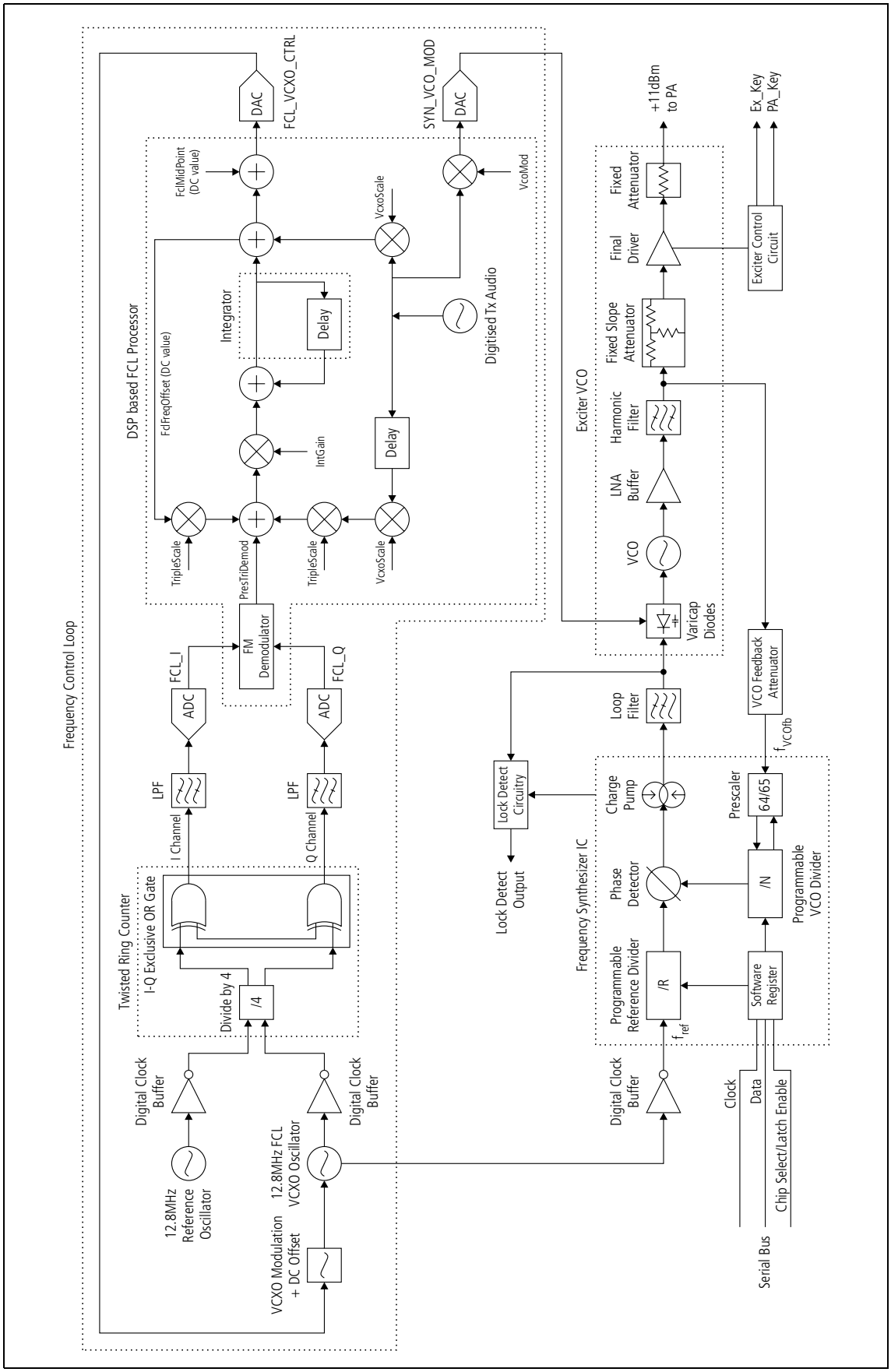
6.3.2 Synthesizer

The exciter synthesizer consists of a programmable frequency synthesizer IC, the exciter VCO, and a modulatable frequency reference.

The synthesizer uses a phase-locked loop to lock the exciter VCO to a modulatable frequency reference. The synthesizer IC receives the divider and control information from the RISC processor via a 3-wire serial bus (clock, data and enable). When the data bits are latched in, the synthesizer processes the incoming signals from the VCO feedback signal (f_{vcofb}) and the reference oscillator (f_{ref}).

The VCO feedback attenuator is a resistive divider that terminates the VCO feedback signal in a fixed low impedance (50Ω). This attenuates the VCO RF level down to a level suitable for the RF prescaler (within the synthesizer IC).

Figure 6.5 Reciter Exciter Synthesizer Modulator Block Diagram - B and H Bands



The FCL_VCXO reference oscillator is modulated by the FCL. The FCL itself is locked to an internal reference 12.8MHz TCXO. When the TCXO is active, the exciter synthesizer is locked to an "internal reference mode" (by default). Alternatively, the FCL is locked to a phase locked 12.8MHz external reference oscillator. When this external oscillator is active, the exciter synthesizer is locked to an "external reference mode". In operation only one reference oscillator is active at any given time. Refer to "Reference Switch" on page 29 for details on the phase-locked 12.8MHz external reference oscillator.

The FCL_VCXO reference oscillator is buffered and divided down to the appropriate divider reference within the synthesizer IC:

- VHF - 3.125kHz (default) or 2.5kHz
- UHF - 6.25kHz (default) or 5kHz.

The same divider reference is maintained by dividing the VCO feedback signal using the prescaler and programmable dividers of the synthesizer IC. Phase lock is achieved when both divider references have same phase and frequency content (i.e. their difference is zero or DC). This is achieved by the phase detector (part of the synthesizer IC), which compares both divider references and delivers an error signal. A ±4mA charge pump circuit (also part of the synthesizer IC) and the active loop filter circuit convert this error signal to a DC voltage (0 to 22V[1]) to tune the VCO for correction. The loop filter has a bandwidth of 150Hz and filters the VCO control lines, reference side bands and spurious signals.

Note The VCO frequency increases as the control line voltage increases.

6.3.3 VCO - VHF Reciter

The exciter VCO consists of a high Q VCO, modulation based on varicap diodes, low noise amplifier, harmonic filter, fixed slope attenuator, final driver and a fixed attenuator.

High Q VCO

The VCO BJT transistor operates in a common emitter, Colpitts oscillator configuration (virtual ground at the base). The LC resonator is coupled between the collector and base. A high Q trimmer is coupled to the base end, and varactor diodes are coupled to the collector end. This forms a high Q resonator which is both mechanically and electronically tunable. Mechanical tuning is possible by adjusting the trimmer. Changes in the control voltage from the loop filter are applied to the varactors to facilitate electronic tuning.

1. The normal lock range is between 3V and 16V.

Modulation Based on Varicap Diodes

Modulation on the VCO is provided by an auxiliary varicap-based control circuit which provides a modulation gain of 5kHz/V_p.

Low Noise Amplifier

A BJT cascode amplifier is used as a broad band isolator and low noise amplifier. This has internal self-bias circuitry, and the output provides enough RF power to drive the following stages.

Harmonic Filter

The VCO has a relatively high harmonic content. A third order low pass elliptic filter is used to attenuate this content.

Fixed Slope Attenuator, Final Driver and Fixed Attenuator

A silicon BJT is used as a broad band matched Class A final driver to drive the +20dBm local oscillator port of the mixer. To maintain a fixed output level, a fixed slope attenuator is introduced at the input to the final driver so that the attenuation rate (slope) increases with an increase in frequency. A fixed attenuator provides a signal level of +11dBm ±2dB to the input port of the PA, providing better reverse isolation.

The B band VCO frequency spans from either 136MHz to 156MHz, or 148MHz to 174MHz, according to the product type.

6.3.4 VCO - UHF Reciter

The exciter VCO consists of a high Q VCO, modulation based on varicap diodes, low noise amplifier, harmonic filter, fixed slope attenuator, final driver and a fixed attenuator.

High Q VCO

The VCO BJT transistor operates in a common collector, Colpitts oscillator configuration, and uses a shorted quarter-wave ceramic coaxial resonator. The open end of the resonator is terminated by a combination of a high Q trimmer and varactor diodes. This forms a high Q resonator which is both mechanically and electronically tunable. Mechanical tuning is possible by adjusting the trimmer. Changes in the control voltage from the loop filter are applied to the varactors to facilitate electronic tuning.

Modulation Based on Varicap Diodes

Modulation on the VCO is provided by an auxiliary varicap-based control circuit which provides a modulation gain of 5kHz/V_p.

Low Noise Amplifier

An N-channel dual gate MOSFET is used as a broad band matched Class A low noise amplifier. It has internal self-bias circuitry, and the output provides enough RF power to drive the following stages.

Harmonic Filter

The VCO has a high second harmonic content. A third order low pass elliptic filter is used to attenuate this content.

Fixed Slope Attenuator, Final Driver and Fixed Attenuator

To provide a drive of +20dBm, a silicon-based BJT transistor is used as a broad band matched Class A final driver. To maintain a fixed input level, a fixed slope attenuator is introduced at the input to the final driver so that the attenuation rate (slope) decreases with an increase in frequency. A fixed attenuator provides a signal level of +11dBm ±2dB to the input port of the PA, providing better reverse isolation.

The H band VCO frequency spans from either 400MHz to 440MHz, 440MHz to 480MHz, or 470MHz to 520MHz, according to the product type.

6.3.5 Exciter Control Circuit

This circuit powers up and shuts down the exciter final driver in a controlled manner. The exciter needs to power up and shut down in a specified time sequence during transient and cyclic keying conditions to reduce the adjacent channel power. The exciter control circuit uses Ex_Key to power up or shut down the VCO final driver, and PA_Key to power up or shut down the PA driver.

7 Power Supply

The reciter is designed to operate from the +28V regulated supply provided by the PMU. The nominal +28V supply enters the reciter digital PCB and passes through an overcurrent and overvoltage protection section before being distributed. The protected +28V output supplies the control comparators, fan switch, and main regulators. There is one regulator on the digital PCB and another on the RF PCB.

7.1 RF PCB

The main regulator is a switched mode converter that has two outputs: the flyback portion generates +8.5V, and the buck portion generates +5.3V.

The +8.5V supply is regulated to +8.0V for reticulation to the RF circuits, either directly, or via switching circuits used in power saving modes. The +8.5V supply is also used to power the analog sections of the network PCB (via the digital PCB).

The +5.3V supply is regulated to +3.3V to power the RF synthesizers.

The RF PCB has a charge pump converter that generates +23V from both the +5.3V and +8.5V supplies. This is used to supply the active loop filters of the RF synthesizers. The +8.5V output and the +5.3V supply to the charge pump can be switched as part of the power saving modes.

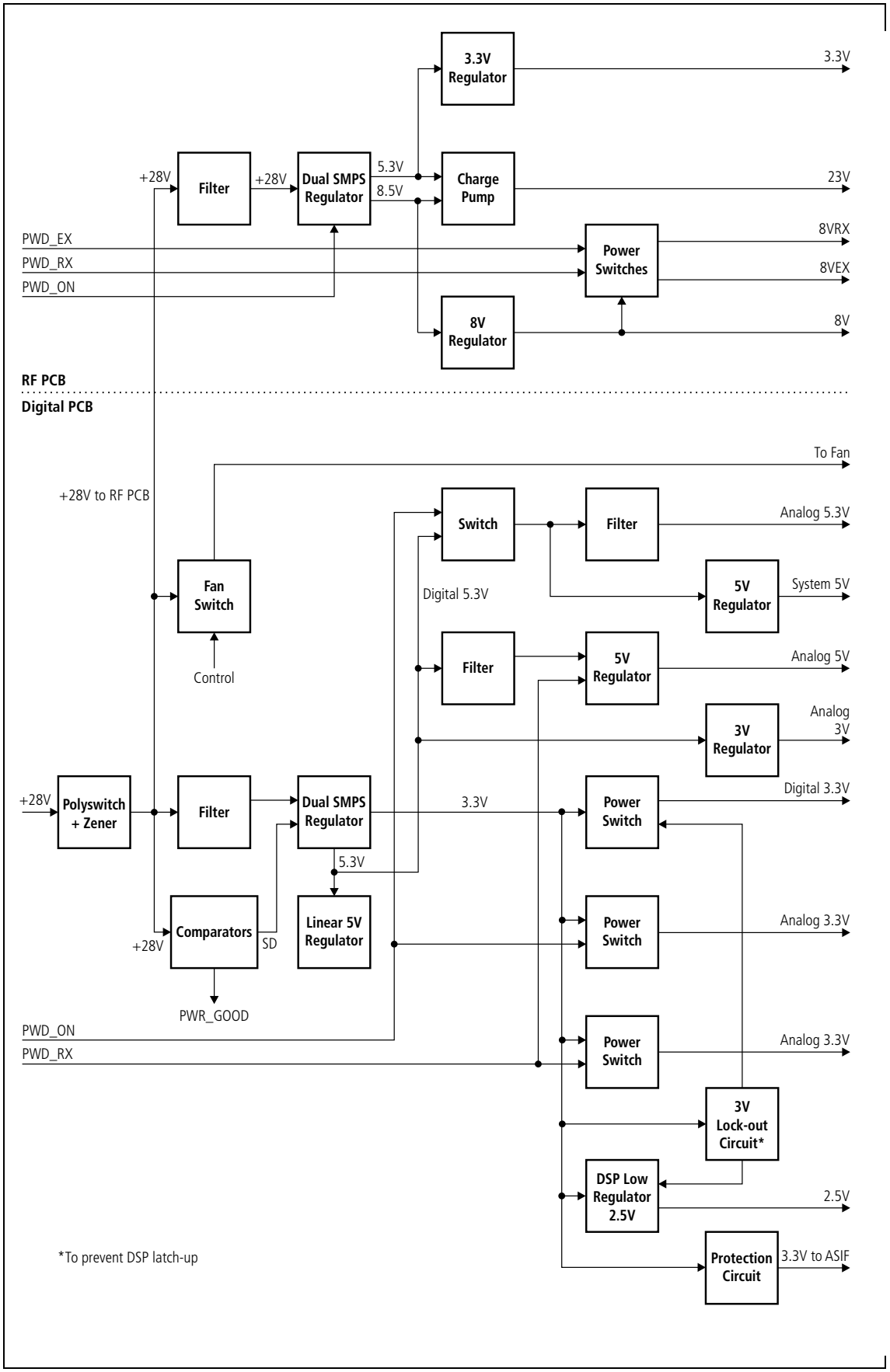
7.2 Digital PCB

The main regulator is a switched mode converter that has two outputs: the flyback portion generates +5.3V, and the buck portion generates +3.3V.

The +5.3V output supplies the op amps associated with the CODECs and is distributed with regulators: +5V for the ADC, +5V for the system, and +3V for the 40MHz clock circuitry. The +5.3V and +5V regulated supplies can be switched as part of the power saving modes.

The +3.3V output is distributed to the remaining circuitry and to the +2.5V regulator for the DSP. These are switched as part of the power saving modes. The +3.3V output is also supplied to the network PCB via a protection circuit.

Figure 7.1 Reciter Power Supply Block Diagram



8 Appendices

8.1 Appendix A – I²C Device Addresses

Table 8.1 I²C Device Addresses

Device	I²C Address Range
U202, 24C16 E2PROM	0xA0 - 0xAF
U500, TLV320AIC1103 CODEC	0xE2 - 0xE3

8.2 Appendix B – ASIF Connectors

Note All signal directions are specified with respect to the ASIF.

8.2.1 J100 MPC859T BDM (Background Debug Mode) Connector

Table 8.2 MPC859T BDM Connector Pinout

Pin Number	Signal Name	Direction	Function
1	VFLS0	O/P	Flush buffer status
2	$\overline{\text{SRESET}}$	I/O	Soft reset
3	GND		
4	DSCK	I/P	Debug serial clock
5	GND		
6	VFLS1	O/P	Flush buffer status
7	$\overline{\text{HRESET}}$	I/O	Hard reset
8	DSDI	I/P	Debug serial data in
9	+3V3		
10	DSDO	O/P	Debug serial data out

8.2.2 J101 ASIF to Reciter Connector

Table 8.3 ASIF to Reciter Connector Pinout

Pin Number	Signal Name	Direction	Function
1	+28V	I/P	Main power input
2	GND		
3	Not used		
4	GND		
5	Not used		
6	GND		
7	SIF_3V3	I/P	Power sense/power supply from reciter
8	GND		
9	PWR_ON	I/P	Reciter power status
10	PWR_RX	I/P	Receiver power status
11	PWR_EX	I/P	Exciter power status
12	GND		

Table 8.3 ASIF to Reciter Connector Pinout (Continued)

Pin Number	Signal Name	Direction	Function
13	RISC_RS232_TXD	I/P	Serial comms input
14	RISC_RS232_RXD	O/P	Serial comms output
15	TX_KEY	O/P	Transmit enable
16	RX_GATE	I/P	Receiver active
17	COAX_RLY_DRV	I/P	Antenna relay control
18	HS_DIG_IN_0	O/P	Reciter digital input
19	HS_DIG_IN_1	O/P	Reciter digital input
20	HS_DIG_IN_2	O/P	Reciter digital input
21	SIO_CLK	I/P	Serial expansion interface clock
22	SIO_TXD	I/P	Serial expansion interface transmit data
23	SIO_RXD	O/P	Serial expansion interface receive data
24	SIO_CON	I/P	Serial expansion interface control/select
25 to 28	Not used		
29	GND		
30 to 37	Not used		
38	RSSI+	I/P	Analog RSSI input
39	RSSI-	I/P	Analog RSSI input
40	Not used		

8.2.3 J102 ASIF DSP to Reciter DSP Connector

Table 8.4 ASIF DSP to Reciter DSP Connector Pinout

Pin Number	Signal Name	Direction	Function
1	Not used		
2	GND		
3	Not used		
4	GND		
5	Not used		
6	GND		
7	Not used		
8	GND		
9	DSP_DT2	I/P	DSP receive data
10	GND		
11	DSP_TCLD2	I/P	DSP receive clock
12	GND		
13	DSP_TFS2	I/P	DSP receive frame sync
14	GND		
15	DSP_DR2	O/P	DSP transmit data
16	GND		
17	DSP_RCLK2	I/P	DSP transmit clock
18	GND		
19	DSP_RSF2	I/P	DSP transmit frame sync
10	GND		
21	DSP_SIF_INT	O/P	1 PPS interrupt

8.2.4 J103 External I/O Connector

Table 8.5 External I/O Connector Pinout

Pin Number	Signal Name	Direction	Function
1	ANT_RLY-DIG4_IN	I/)	Antenna relay control O/P, general purpose digital I/P
2	RS232_TXD	O/P	Serial comms O/P
3	RS232_RXD	I/P	Serial comms I/P
4	DIG0_IN	I/P	General-purpose digital input
5	GND		
6	DIG1_IN	I/P	General-purpose digital input
7	DIG2_IN	I/P	General-purpose digital input
8	DIG3_IN	I/P	General-purpose digital input
9	RSSI_OUT	O/P	Analog RSSI O/P, general-purpose digital I/O

8.2.5 J104 Ethernet Connector

Table 8.6 Ethernet Connector Pinout

Pin Number	Signal Name	Direction	Function
1	TX+	O/P	Transmit signal
2	TX-	O/P	Transmit signal
3	RX-	O/P	Receive signal
4	Not used		
5	Not used		
6	RX-	I/P	Receive signal
7	Not used		
8	Not used		

8.2.6 J105 4W Audio and E&M Connector

Table 8.7 4W Audio and E&M Connector Pinout

Pin Number	Signal Name	Direction	Function
1	Ea	I/P	Signaling input
2	Eb	I/P	Signaling input
3	Ta	O/P	4W audio output
4	Tb	O/P	4W audio output
5	Ra	I/P	4W audio input
6	Rb	I/P	4W audio input
7	Ma	O/P	Signaling output
8	Mb	O/P	Signalling output

8.2.7 J106 DSP JTAG Connector (on underside of board)

Table 8.8 DSP JTAG Connector Pinout

Pin Number	Signal Name	Direction	Function
1	TMS	I/P	Test mode select
2	TRST	I/P	Test mode reset
3	TDI	I/P	Test data input
4	GND		
5 to 6	Not used		
7	TDO	I/P	Test data output
8	GND		
9	TCK_RETURN	O/P	Test clock output
10	GND		
11	TCK	I/P	Test clock input
12	EMU0	I/P	Emulation mode select
13	Not used		
14	EMU1	I/P	Emulation mode select

8.3 Appendix C – Test Points

Table 8.9 Testpoints

Reference Designator	PCB Grid Reference	Function
TP200	A4	General-purpose software flag
TP201	A6	General-purpose software flag
TP202	A4	CPU instruction watchpoint flag - IWP2
TP203	A2	CPU load/store watchpoint flag - LWP1
TP204	A3	CPU address type output - AT3
TP205	A5	JTAG test mode select - TMS
TP206	A6	General-purpose software flag
TB207	A2	CPU address type output - AT2
TP208	A5	CPU load/store watchpoint flag - LWP0
TP209	A2	CPU address type output - AT0
TB210	A3	Flash memory chip select -
TP211	A3	SDRAM memory chip select -
TP212	A4	SDRAM write enable -
TP213	C6	Memory clock
TP214	A3	SDRAM column address strobe -
TP215	A5	SDRAM row address strobe -
TP216	A4	SDRAM byte select -
TP217	A5	SDRAM byte select -
TP218	A6	SDRAM byte select -
TP219	A6	SDRAM byte select -
TP220	A1	DSP chip select -
TP221	A1	Software strobe output
TP222	A1	DSP write enable -
TP223	A2	Transfer acknowledge -
TP400	E3	General-purpose DSP software flag
TP401	E3	General-purpose DSP software flag
TP402	E3	General-purpose DSP software flag
TP403	D3	General-purpose DSP output flag -
TP404	F3	General-purpose DSP software flag
TP405	E3	General-purpose DSP software flag
TP406	E2	DSP serial port transmit data -

Table 8.9 Testpoints (Continued)

Reference Designator	PCB Grid Reference	Function
TP407	D2	DSP serial port transmit frame sync
TP408	E2	DSP serial port transmit clock -
TP409	E2	DSP serial port receive frame sync -
TP410	E2	DSP serial port receive clock -
TP411	F3	DSP serial port receive data -
TP412	E5	DSP clock output
TP413	D2	DSP host port ready output - HRDY
TP900	N78	Ground
TP910	A18	Ground

8.4 Appendix D – Processor Port Assignments

8.4.1 MPC859T Port Assignments

Note Many of the pins on the MPC859T have multiple functions. Where a particular pin function is used in the ASIF application, this is indicated in bold text; unused functions or unused pins are in plain text. This table is sorted by pin name order; where a pin has multiple function names, these are listed in the order shown on the schematic. This table also lists the UTOPIA interface pin names, but, for clarity, these are not shown on the schematic.

Table 8.10 MPC859T Port Assignments

Pin Name	Pin No.	Type	Function
A[0]	B19	I/O	Address bus 0 - msb
A[1]	B18	I/O	Address bus 1
A[2]	A18	I/O	Address bus 2
A[3]	C16	I/O	Address bus 3
A[4]	B17	I/O	Address bus 4
A[5]	A17	I/O	Address bus 5
A[6]	B16	I/O	Address bus 6
A[7]	A16	I/O	Address bus 7
A[8]	D15	I/O	Address bus 8
A[9]	C15	I/O	**Address bus 9**
A[10]	B15	I/O	**Address bus10**
A[11]	A15	I/O	**Address bus 11**
A[12]	C14	I/O	**Address bus 12**
A[13]	B14	I/O	**Address bus 13**
A[14]	A14	I/O	**Address bus 14**
A[15]	D12	I/O	**Address bus 15**
A[16]	C13	I/O	**Address bus 16**
A[17]	B13	I/O	**Address bus 17**
A[18]	D9	I/O	**Address bus 18**
A[19]	D11	I/O	**Address bus 19**
A[20]	C12	I/O	**Address bus 20**
A[21]	B12	I/O	**Address bus 21**
A[22]	B10	I/O	**Address bus 22**
A[23]	B11	I/O	**Address bus 23**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
A[24]	C11	I/O	**Address bus 24**
A[25]	D10	I/O	**Address bus 25**
A[26]	C10	I/O	**Address bus 26**
A[27]	A13	I/O	**Address bus 27**
A[28]	A10	I/O	**Address bus 28**
A[29]	A12	I/O	**Address bus 29**
A[30]	A11	I/O	**Address bus 30**
A[31]	A9	I/O	**Address bus 31**
ALEA MIITXD1	K2	O/P	Address Latch Enable A MII Transmit Data 1
ALEB DSCK AT1	JI	I/O	Address Latch Enable B Development Serial Clock Address Type 1
$\overline{AS}$	L3	I/P	Address Strobe
BADDR28	M3	O/P	Burst Address [28]
BADDR29	M2	O/P	Burst Address [29]
BADDR30 $\overline{REG}$	K4	O/P	Burst Address [30} Register select
$\overline{BB}$	E1	I/O	Bus Busy
$\overline{BDIP}$ $\overline{GPL\_B5}$	D2	O/P	Burst Data In Progress General-purpose Line B5
$\overline{BG}$	E2	I/O	Bus Grant
$\overline{BI}$	E3	I/O	Burst Inhibit
$\overline{BR}$	G4	I/O	Bus Request
BRGO1 **I2CSDA** PB27	E19	I/O	BRG1 output clock **I^2C serial data pin** General-purpose I/O port B, bit 27
BRGO2 **I2CSCL** PB26	F19	I/O	BRG2 output clock **I^2C serial clock pin** General-purpose I/O port B, bit 26
BRGO3 **PB15** Txclav	R17	I/O	BRG3 output clock **General-purpose I/O port B, bit 15** Transmit cell available input signal
BRG04 **SPIMOSI** PB28	D19	I/O	BRG4 output clock SPI output data in server mode; **SPI input data in client mode** General-purpose I/O port B, bit 28
$\overline{BS\_A0}$	D8	O/P	**Byte Select 0 on UPMA**
$\overline{BS\_A1}$	C8	O/P	**Byte Select 1 on UPMA**
$\overline{BS\_A2}$	A7	O/P	**Byte Select 2 on UPMA**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
$\overline{\text{BS\_A3}}$	B8	O/P	**Byte Select 3 on UPMA**
$\overline{\text{BURST}}$	F1	I/O	Burst transaction
$\overline{\text{CE1A}}$ MIITXD2	B3	O/P	Card Enable 1 Slot A MII transmit data 2
$\overline{\text{CE2A}}$ MIITXD3	A3	O/P	Card Enable 2 Slot A MII transmit data 3
CLKOUT	**W3**	**O/P**	**Clock Output**
$\overline{\text{CSO}}$	**C3**	**O/P**	**Chip Select 0**
$\overline{\text{CS1}}$	**A2**	**O/P**	**Chip Select 1**
$\overline{\text{CS2}}$	**D4**	**O/P**	**Chip Select 2**
$\overline{\text{CS3}}$	E4	O/P	Chip Select 3
$\overline{\text{CS4}}$	A4	O/P	Chip Select 4
$\overline{\text{CS5}}$	B4	O/P	Chip Select 5
$\overline{\text{CS6}}$ $\overline{\text{CE1B}}$	D5	O/P	Chip Select 6 Card Enable 1 Slot B
$\overline{\text{CS7}}$ $\overline{\text{CE2B}}$	C4	O/P	Chip Select 7 Card Enable 2 Slot B
$\overline{\text{CTS1}}$ PC11	J19	I/O	Clear to send modem line for SCC1 General-purpose I/O port C, bit 11
D[0]	W14	I/O	**Data Bus 0 - msb**
D[1]	W12	I/O	**Data Bus 1**
D[2]	W11	I/O	**Data Bus 2**
D[3]	W10	I/O	**Data Bus 3**
D[4]	W13	I/O	**Data Bus 4**
D[5]	W9	I/O	**Data Bus 5**
D[6]	W7	I/O	**Data Bus 6**
D[7]	W6	I/O	**Data Bus7**
D[8]	U13	I/O	**Data Bus 8**
D[9]	T11	I/O	**Data Bus 9**
D[10]	V11	I/O	**Data Bus 10**
D[11]	U11	I/O	**Data Bus 11**
D[12]	T13	I/O	**Data Bus 12**
D[13]	V13	I/O	**Data Bus 13**
D[14]	V10	I/O	**Data Bus 14**
D[15]	T10	I/O	**Data Bus 15**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
D[16]	U10	I/O	**Data Bus 16**
D[17]	T12	I/O	**Data Bus 17**
D[18]	V9	I/O	**Data Bus 18**
D[19]	U9	I/O	**Data Bus 19**
D[20]	V8	I/O	**Data Bus 20**
D[21]	U8	I/O	**Data Bus 21**
D[22]	T9	I/O	**Data Bus 22**
D[23]	U12	I/O	**Data Bus 23**
D[24]	V7	I/O	**Data Bus 24**
D[25]	T8	I/O	**Data Bus 25**
D[26]	U7	I/O	**Data Bus 26**
D[27]	V12	I/O	**Data Bus 27**
D[28]	V6	I/O	**Data Bus 28**
D[29]	W5	I/O	**Data Bus 29**
D[30]	U6	I/O	**Data Bus 30**
D[31]	T7	I/O	**Data Bus 31 - lsb**
DPO **$\overline{\text{IRQ3}}$**	V3	I/O	Data Parity 0 **Interrupt Request 3**
DP1 **$\overline{\text{IRQ4}}$**	V5	I/O	Data Parity 1 **Interrupt Request 4**
DP2 $\overline{\text{IRQ5}}$	W2	I/O	Data Parity 2 Interrupt Request 5
DP3 **$\overline{\text{IRQ6}}$**	V4	I/O	Data Parity 3 **Interrupt Request 6**
EXTAL	N1	I/P	Crystal oscillator input
EXTCLK	N2	I/P	**External clock input**
FRZ $\overline{\text{IRQ6}}$	G3	I/O	Freeze Interrupt Request 6
$\overline{\text{GPLA0}}$ $\overline{\text{GPLB0}}$	D7	O/P	**General-purpose Line 0 on UPMA** General-purpose Line 0 on UPMB
$\overline{\text{GPLA1}}$ $\overline{\text{OE}}$ $\overline{\text{GPLB1}}$	C6	O/p	**General-purpose Line 1 on UPMA** Output Enable General-purpose Line 1 on UPMB
$\overline{\text{GPLA2}}$ GPLB2 $\overline{\text{CS2}}$	B5	O/P	**General-purpose Line 2 on UPMA** General-purpose Line 2 on UPMB Chip Select 2

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
$\overline{\text{GPLA3}}$ GPLB3 $\overline{\text{CS3}}$	C5	O/P	**General-purpose Line 3 on UPMA** General-purpose Line 3 on UPMB Chip Select 3
$\overline{\text{GPLZA5}}$	D3	O/P	General-purpose Line 5 on UPMA
$\overline{\text{HRESET}}$	N4	I/O	**Hard Reset**
IPA0 MIIRXD3 UTPB_Split[0]	T5	I/P	**Input Port A[0]** MII Receive data 3 UTOPIA Split Bus [0]
IPA1 MIIRXD2 UTPB_Split[1]	T4	I/P	**Input Port A[1]** MII Receive data 2 UTOPIA Split Bus [1]
IPA2 IOS16A MIIRXD1 UTPB_Split[2]	U3	I/P	**Input Port A[2]** I/O Device A is 16 bits MII Receive data 1 UTOPIA Split Bus [2]
IPA3 MIIRXD0 UTPB_Split[3]	W2	I/P	**Input Port A[3]** MII Receive data 0 UTOPIA Split Bus [3]
IPA4 MIIRXCLK UTPB_Split[4]	U4	I/P	**Input Port A[4]** MII Receive Clock UTOPIA Split Bus [4]
IPA5 MIIRXERR UTPB_Split[5]	U5	I/P	**Input Port A[5]** MII Receive Error UTOPIA Split Bus [5]
IPA6 MIITXERR UTPB_Split[6]	T6	I/O	**Input Port A[6]** MII Transmit Error UTOPIA Split Bus [6]
IPA7 MIIRXDV UTPB_Split[7]	T3	I/P	**Input Port A[7]** MII Receive Data Valid UTOPIA Split Bus [7]
IPB0 IWP0 **VFLS0**	H2	I/O	Input Port B[0] Instruction Watchpoint 0 **Visible History Buffer Flush Status 0**
IPB0 IWP0 **VFLS0**	H2	I/O	Input Port B[0] Instruction Watchpoint **Visible History Buffer Flush Status 0**
IPB2 IOIS16B **AT2**	J2	I/O	Input Port B[2] I/O Device B is 16 bits port size **Address Type 2**
IPB3 IWP2 **VF2**	G1	I/O	Input Port B[3] Instruction Watchpoint 2 **Visible Instruction Queue Flush Status 2**
IPB4 LWP0 **VF0**	G2	I/O	Input Port B[4] Load/Store Watchpoint 0 **Visible Instruction Queue Flush Status 0**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
IPB5 LWP1 **VF1**	J4	I/O	Input Port B[5] Load/Store Watchpoint 1 **Visible Instruction Queue Flush Status 1**
IPB6 DSD1 **AT0**	K3	I/O	Input Port B[6] Development Serial Data Input **Address Type 0**
IPB7 $\overline{\text{PTR}}$ **AT3**	H1	I/O	Input Port B[7] Program Trace **Address Type 3**
$\overline{\text{IRQ0}}$	V14	I/P	Interrupt Request 0
$\overline{\text{IRQ1}}$	U14	I/P	Interrupt Request 1
$\overline{\text{IRQ2}}$ $\overline{\text{RSV}}$	H3	I/P	Interrupt Request 0 Reservation
$\overline{\text{IRQ3}}$ $\overline{\text{CR}}$	H2	I/P	Interrupt Request 3 Cancel Reservation
$\overline{\text{IRQ4}}$ $\overline{\text{KR}}$ $\overline{\text{RETRY}}$ SPKROUT	K1	I/O	Interrupt Request 4 Kill Reservation Retry Speaker Out
$\overline{\text{IRQ7}}$ **MTXCLK**	W15	I/O	Interrupt Request 7 **MII Transmit Clock**
L1CLKRB TOUT3 CLK6 **PA2**	R18	I/O	Receive clock for the serial interface TDMb Timer 3 output Clock input for SCCs and SMCs or BRG clock **General-purpose I/O port A, bit 2**
L1RSYNCA PC4	T17	I/O	**Receive sync input for serial interface TDMa** General-purpose I/O port C, bit 4
L1RxDA PA8	L17	I/O	**Receive data input for the serial interface TDMa** General-purpose I/O Port A, bit 8
L1RxDB PA10	J17	I/O	Receive data input for the serial interface TDMb General-purpose I/O Port A, bit 10
L1ST1 RTSI1 **PB19**	N19	I/O	Output strobe from the serial interface. Request to send modem line for SCC1 **General-purpose I/O Port B, bit 19**
L1ST2 DREQ1 **PC14**	D18	I/O	Output strobe from the serial interface IDMA channel 2 request input **General-purpose I/O port C, bit 14**
L1ST2 **PB18** RXADDR4	n17	I/O	Output strobes from the serial interface **General-purpose I/O Port B, bit 18** UTOPIA multi-PHY receive address line 4
L1ST3 L1RQb **PB17** PHREQ[1] RXADDR1	P18	I/O	Output strobe from the serial interface D-channel request signal for serial interface TDMb **General-purpose I/O port B, bit 17** Least significant bit of PHY request bus UTOPIA multi-PHY receive address line 1

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
L1ST3 L1RQb **PC13**	E18	I/O	Output strobe from the serial interface D-channel request signal for serial interface TDMb **General-purpose I/O port C, bit 13**
L1ST4 L1RQA **PB16** PHREQ[0] RXADDR0	N16	I/O	Output strobe from the serial interface D-channel request signal for serial interface TDMa **General-purpose I/O port B, bit 16** Most significant bit of PHY request bus UTOPIA multi-PHY receive address line 0
L1ST4 L1Rqa **PC12**	F18	I/O	Output strobes from the serial interface D-channel request signal for serial interface TDMa. **General-purpose I/O port C, bit 12**
L1SYNCB PC6	R19	I/O	Receive sync input for the serial interface TDMb General-purpose I/O port C, bit 6
L1TCLKB TOUT4 CLK8 **PA0**	U19	I/O	Transmit clock for the serial interface TDMb Timer 4 output Clock input for SCCs and SMCs. **General-purpose I/O port A, bit 0**
L1TSYNCB PC7 SDACK2	M16	I/O	Transmit sync input for serial interface TDMb General-purpose I/O port C, bit 7 SDMA acknowledge 2 output
L1TxDA PA9	K18	I/O	**Transmit data O/P for the serial interface TDMa** General-purpose I/O Port A, bit 9
L1TxDB **PA11**	G16	I/O	Transmit data O/P for serial interface TDMb **General-purpose I/O port A, bit 11**
MII_MDIO	H18	I/O	**MII management data**
MII_COL	H4	I/P	**MII collision**
MII_CRS	B7	I/P	**Input MII carrier receive sense**
MIIMDC L1RSYNCB PD12 UTPB[3]	R16	I/O	**Media independent interface management data clock** Input receive data sync signal to TDM channel B General-purpose I/O port D, bit 12 UTOPIA bus bit 3 input/output signal
MIIRXCLK MIIMDC PD8	W17	I/O	**Media independent interface receive clock** Media independent interface management data clock General-purpose I/O port D, bit 8
MIIRXD0 PD10 TXENB	W18	I/O	**Media independent interface receive data 0** General-purpose I/O port D, bit 10 Transmit enable output signal
MIIRXD1 L1TSYNCB PD13 UTPB[2]	V18	I/O	**Media independent interface receive data 1** Input transmit data sync signal to TDM channel B General-purpose I/O port D, bit 13 UTOPIA bus bit 2 input/output signal
MIIRXD2 L1RSYNCA PD14 UTPB[1]	V19	I/O	**Media independent interface receive data 2** Input receive data sync signal to TDM channel A General-purpose I/O port D, bit 14 UTOPIA bus bit 1 input/output signal

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
MIIRXD3 L1TSYNCA PD15 UTPB[0]	U17	I/O	**Media independent interface receive data 3** Input transmit data sync signal to TDM channel A General-purpose I/O port D, bit 15 UTOPIA bus bit 0 input/output signal
MIIRXDV PD6 UTPB[5]	V16	I/O	**Media independent interface receive data valid** General-purpose I/O port D, bit 6 UTOPIA bus bit 5 input/output signal
MIIRXERR PD7 UTPB[4]	T15	I/O	**Media independent interface receive error** General-purpose I/O port D, bit 7 UTOPIA bus bit 4 input/output signal
MIITXD0 PD9 UTPCLK	V17	I/O	**Media independent interface transmit data 0** General-purpose I/O port D, bit 9 UTOPIA Clock input/output signal
MIITXD1 PD3 SOC	W16	I/O	**Media independent interface transmit data 1** General-purpose I/O Port D Bit 3 Start of cell input/output signal
MIITXD2 PD4 UTPB[7]	U16	I/O	**Media independent interface transmit data 2** General-purpose I/O Port D Bit 4 UTOPIA bus bit 7 input/output signal. (most significant bit of UTPB)
MIITXD3 PD5 UTPB[6]	U15	I/O	**Media independent interface transmit data 3** General-purpose I/O port D, bit 5 UTOPIA bus bit 6 input/output signal
MII_TXEN	V15	O/P	**MII transmit enable**
MIITXERR PD11 RXENB	T16	I/O	**Media independent interface transmit error** General-purpose I/O port D, bit 11 Receive enable output signal
OP0 MIITXD0 UtpClk_Split	L4	O/P	Output Port 0 MII Transmit Data 0 UTOPIA Clock Split
OP1	L2	O/P	Output Port 1
OP2 **MODCK1** STS	L1	I/O	Output Port 2 **Mode Clock 1** Special Transfer Start
OP3 **MODCK2** DSD0	M4	I/O	Output Port 3 **Mode Clock 2** Development Serial Data Output
PA12	F17	I/O	**General-purpose I/O port A, bit 12**
PA13	E17	I/O	**General-purpose I/O port A, bit 13**
PB22 TXADDR4	L19	I/O	**General-purpose I/O port B, bit 22** UTOPIA multi-PHY transmit address line 4
PC9	L18	I/O	General-purpose I/O port C, bit 9
$\overline{\text{PORESET}}$	R2	I/P	**Power-on Reset**
RD/$\overline{\text{WR}}$	B2	I/O	**Read/Write**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
REJECT1 **SPISEL** PB31	C17	I/O	SCC1 CAM interface reject pin **SPI client select input** General-purpose I/O port B, bit 31
RSTCONF	P3	I/P	Reset Configuration
RSTRT1 **PB14** RXADDR2	U18	I/O	SCC1 serial CAM interface outputs that marks the start of a frame **General-purpose I/O port B, bit 14** UTOPIA multi-PHY receive address line 2
L1ST1 RTS1 DREQ0 **PC15** Rxclav	D16	I/O	Output strobes from the serial interface Request to send modem line for SCC1 IDMA channel 1 request input **General-purpose I/O port C, bit 15** Receive cell available input signal
RxD1 PA15	D17	I/O	**SCC1 Receive Data input** General-purpose I/O port A, bit 15
SDACK1 **L1TSYNCA** PC5	T18	I/O	SDMA acknowledge 1output **Transmit sync input for serial interface TDMa** General-purpose I/O port C, bit 5
SMRxD1 PB24 TXADDR3	J18	I/O	**SMC1 receive data input** General-purpose I/O port B, nit 24 UTOPIA multi-PHY transmit address line 3
SMRxD2 L1CLKOA **PB20** PHSEL[0] TXADDR0	L16	I/O	SMC2 receive data input Clock output from the serial interface TDMa **General-purpose I/O port B, bit 20** Most significant bit of PHY select bus UTOPIA multi-PHY transmit address line 0
SMSYN1 SDACK1 **PB23** TXADDR2	K17	I/O	SMC1 external sync input SDMA acknowledge **General-purpose I/O port B, bit 23** UTOPIA multi-PHY transmit address line 2
SMTxD1 PB25 RXADDR3	J16	I/O	**SMC1 transmit data output** General-purpose I/O port B, bit 25 UTOPIA multi-PHY receive address line 3
SMTxD2 L1CLKOB **PB21** PHSEL[1] TXADDR1	K16	I/O	SMC2 transmit data output Clock output from the serial interface TDMb **General-purpose I/O port B, bit 21** Least significant bit of PHY select bus UTOPIA multi-PHY transmit address line 1
SPICLK PB30	C19	I/O	**SPI output clock in server mode or SPI input clock in client mode** General-purpose I/O port B, bit 30
SPIMOSI PB29	E16	I/O	**SPI output data in server mode or SPI input data in client mode** General-purpose I/O port B, bit 29
$\overline{\text{SRESET}}$	P2	I/O	**Soft Reset**
$\overline{\text{TA}}$	C2	I/O	**Transfer Acknowledge**
TCK **DSCK**	H16	I/P	Provides clock to scan chain logic **Provides clock to the development port logic**

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
TDI **DSDI**	H17	I/P	Input serial data for the scan chain logic **Input serial data for the development port and determines the operating mode of the development port at reset**
TDO **DSDO**	G17	O/P	Output serial data for the scan chain logic **Output serial data for the development port**
$\overline{\text{TEA}}$	D1	I/O	Transfer Error Acknowledge
TEXP	N3	O/P	Timer Expired
TGATE1 CD1 PC10	K19	I/O	Timer 1/timer 2 gate signal Carrier detect modem line for SCC1 General-purpose I/O port C, bit 10
TGATE2 PC8		I/O	Timer 3/timer 4 gate signal General-purpose I/O port C, bit 8
TIN1 **L1RCLKA** BRGO1 CLK1 PA7	M19	I/O	Timer 1 external clock **Receive clock for the serial interface TDMa** Output clock of BRG1 Clock input 1 for SCCs and SMCs General-purpose I/O port A, bit 7
TIN2 **L1TCLKA** BRGO2 CLK3 PA5	N18	I/O	Timer 2 external clock input **Transmit clock for the serial interface TDMa** Output clock of BRG2 Clock inputs for SCCs and SMCs General-purpose I/O port A, bit 5
TIN3 BRGO3 CLK5 PA3	P17	I/O	**Timer 3 external clock input** Output clock of BRG3 Clock inputs for SCCs and SMCs General-purpose I/O port A, bit 3
TIN4 BRGO4 CLK7 **PA1**	T19	I/0	Timer 4 external clock input BRG4 output clock Clock input for SCCs and SMCs **General-purpose I/O port A, bit 1**
TMS	G18	I/P	Controls the scan chain test mode operations
TOUT1 CLK2 PA6	M17	I/O	Timer 1 output Clock input for SCCs and SMCs General-purpose I/O Port A Bit 6
TOUT2 CLK4 **PA4**	P19	I/O	Timer 2 output Clock inputs for SCCs and SMCs **General-purpose I/O Port A, bit 4**
TRST	G19	I/P	**Test reset for the JTAG scan chain logic**
$\overline{\text{TS}}$	F3	1/0	Transfer Start
TSIZ0 $\overline{\text{REG}}$	B9	I/O	Transfer Size 0 Register
TSIZ1	C9	I/O	Transfer Size 1
TxD1 PA14	D17	I/O	**SCC1 Transmit Data** General-purpose I/O port A, bit 14

Table 8.10 MPC859T Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
UPWAITA GPLA4	C1	I/O	User Programmable machine Wait A General-purpose Line 4 on UPMA
UPWAITB GPLB4	B1	I/O	User Programmable machine Wait B General-purpose Line 4 on UPMB
VDDH		PWR	I/O buffers supply voltage
VDDL		PWR	Core logic supply voltage
VDDSYN		PWR	PLL supply voltage
VSS		PWR	Ground
VSSSYN		PWR	PLL ground
VSSSYN1		PWR	PLL ground
WAITA SOC_Split	R3	I/P	Wait Slot A Start of Cell in UTOPIA Split Bus Mode
WAITB	R4	I/P	Wait Slot B
$\overline{\text{WE0}}$ $\overline{\text{BS\_B0}}$ $\overline{\text{IORD}}$	C7	O/P	**Write Enable 0** Byte Select 0 on UPMB I/O Device Read
$\overline{\text{WE1}}$ $\overline{\text{BS\_B1}}$ $\overline{\text{IOWR}}$	A6	O/P	Write Enable 1 Byte Select 1 on UPMB I/O Device Write
$\overline{\text{WE2}}$ $\overline{\text{BS\_B2}}$ $\overline{\text{PCOE}}$	B6	O/P	Write Enable 2 Byte Select 2 on UPMB PCMCIA Output Enable
$\overline{\text{WE3}}$ $\overline{\text{BS\_B3}}$ $\overline{\text{PCWE}}$	A5	O/P	Write Enable 3 Byte Select 3 on UPMB PCMCIA Write Enable
XTAL	P1	O/P	Crystal oscillator output

8.4.2 TMS320VC5510 Port Assignments

Note Used pin are shown in bold text; unused pins in plain text. This table is sorted by pin name order.

Table 8.11 TMS320VC5510 Port Assignments

Pin Name	Pin No.	Type	Function
A[0]	B8	O/P	External memory address bus (byte address) 0
A[1]	D8	O/P	External memory address bus 1
A[2]	B7	O/P	External memory address bus 2
A[3]	C7	O/P	External memory address bus 3
A[4]	A6	O/P	External memory address bus 4
A[5]	C6	O/P	External memory address bus 5
A[6]	C4	O/P	External memory address bus 6
A[7]	C5	O/P	External memory address bus 7
A[8]	A4	O/P	External memory address bus 8
A[9]	A2	O/P	External memory address bus 9
A[10]	C1	O/P	External memory address bus 10
A[11]	E1	O/P	External memory address bus 11
A[12]	F3	O/P	External memory address bus 12
A[13]	F2	O/P	External memory address bus 13
A[14]	G4	O/P	External memory address bus 14
A[15]	G3	O/P	External memory address bus 15
A[16]	F4	O/P	External memory address bus 16
A[17]	G2	O/P	External memory address bus 17
A[18]	H4	O/P	External memory address bus 18
A[19]	H3	O/P	External memory address bus 19
A[20]	J4	O/P	External memory address bus 20
A[21]	J3	O/P	External memory address bus 21
AOE	U15	O/P	Asynchronous memory output enable
ARDY	P13	O/P	Asynchronous memory ready input
ARE	R14	O/P	Asynchronous memory read enable
AWE	T13	O/P	Asynchronous memory write enable
BE0	K2	O/P	Byte-enable control 0
BE1	K3	O/P	Byte-enable control 1
BE2	L3	O/P	Byte-enable control 2
BE3	L4	O/P	Byte-enable control 3

Table 8.11 TMS320VC5510 Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
BOOTM3	E5	I/P	**Boot Mode Selection signal 3**
CE0	J2	O/P	External memory space enable 0
CE1	H2	O/P	External memory space enable 1
CE2	G1	O/P	External memory space enable 2
CE3	E4	O/P	External memory space enable 3
CLKIN	F16	I/P	**Clock input**
CLKMD	P16	I/P	**Clock mode select**
CLKMEM	B9	O/P	Memory interface clock (for SDRAM / SBSRAM
CLKOUT	H15	O/P	**Clock output**
CLKR0	U3	I/P	**Serial shift clock input for McBSP 0**
CLKR1	T3	I/P	**Serial shift clock input for McBSP 1**
CLKR2	R5	I/P	**Serial shift clock input for McBSP 2**
CLKS0	U5	I/P	Ext. clock source to the sample rate generator 0
CLKS1	P2	I/P	Ext. clock source to the sample rate generator 1
CLKS2	P8	I/P	Ext. clock source to the sample rate generator 2
CLKX0	U7	I/O	**Serial shift clock input for McBSP 0**
CLKX1	R15	I/O	**Serial shift clock input for McBSP 1**
CLKX2	U8	I/O	Serial shift clock input for McBSP 2
CVDD		PWR	Dedicated power supply for the internal logic (CPU and peripherals)
D[0]	C8	I/O	External data bus 0
D[1]	D7	I/O	External data bus 1
D[2]	AB	I/O	External data bus 2
D[3]	B6	I/O	External data bus 3
D[4]	D6	I/O	External data bus 4
D[5]	B5	I/O	External data bus 5
D[6]	D5	I/O	External data bus 6
D[7]	B4	I/O	External data bus 7
D[8]	D4	I/O	External data bus 8
D[9]	B3	I/O	External data bus 9
D[10]	C3	I/O	External data bus 10
D[11]	D3	I/O	External data bus 11
D[12]	E3	I/O	External data bus 12
D[13]	C2	I/O	External data bus 13

Table 8.11 TMS320VC5510 Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
D[14]	D2	I/O	External data bus 14
D[15]	E2	I/O	External data bus 15
D[16]	N3	I/O	External data bus 16
D[17]	T1	I/O	External data bus 17
D[18]	R3	I/O	External data bus 18
D[19]	P4	I/O	External data bus 19
D[20]	R4	I/O	External data bus 20
D[21]	T4	I/O	External data bus 21
D[22]	P5	I/O	External data bus 22
D[23]	P6	I/O	External data bus 23
D[24]	P7	I/O	External data bus 24
D[25]	T7	I/O	External data bus 25
D[26]	R8	I/O	External data bus 26
D[27]	T8	I/O	External data bus 27
D[28]	P11	I/O	External data bus 28
D[29]	T9	I/O	External data bus 29
D[30]	T10	I/O	External data bus 30
D[31]	P10	I/O	External data bus 31
DR0	T6	I/P	**Serial receive data input for McBSP 0**
DR1	P3	I/P	**Serial receive data input for McBSP 1**
DR2	R7	I/P	**Serial receive data input for McBSP 2**
DVDD		PWR	Dedicated power supply for the I/O pins
DX0	R10	O/P	**Serial transmit data output for McBSP 0**
DX1	T16	O/P	**Serial transmit data output for McBSP 1**
DX2	U11	O/P	**Serial transmit data output for McBSP 2**
EMU0	R16	I/O	**Emulation pin 0**
EMU1/OFF	L14	I/O	**Emulation pin 1/ disable all outputs**
FSR0	T5	I/O	**Frame synchronisation signal for McBSP 0**
FSR1	R2	I/O	**Frame synchronisation signal for McBSP 1**
FSR2	R6	I/O	**Frame synchronisation signal for McBSP 2**
FSX0	P9	I/O	**Frame synchronisation signal for McBSP 0**
FSX1	T15	I/O	**Frame synchronisation signal for McBSP 1**
FSX2	R9	I/O	**Frame synchronisation signal for McBSP 2**

Table 8.11 TMS320VC5510 Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
HA[0]	D16	I/P	**Host address bus 0**
HA[1]/HCNTL1	E16	I/P	**Host address bus 1**
HA[2]/HAS	F15	I/P	**Host address bus 2**
HA[3]	G15	I/P	**Host address bus 3**
HA[4]	H14	I/P	**Host address bus 4**
HA[5]	J14	I/P	**Host address bus 5**
HA[6]	K17	I/P	**Host address bus 6**
HA[7]	J16	I/P	**Host address bus 7**
HA[8]	G14	I/P	**Host address bus 8**
HA[9]	F14	I/P	**Host address bus 9**
HA[10]	E15	I/P	**Host address bus 10**
HA[11]	D15	I/P	**Host address bus 11**
HA[12]	E14	I/P	**Host address bus 12**
HA[13]	G17	I/P	**Host address bus 13**
HA[14]	H16	I/P	**Host address bus 14**
HA[15]	J15	I/P	**Host address bus 15**
HA[16]	K16	I/P	**Host address bus 16**
HA[17]	M15	I/P	**Host address bus 17**
HA[18]	M14	I/P	**Host address bus 18**
HA[19]	N17	I/P	**Host address bus 19**
HBE0	K15	I/P	HPI byte enable 0
HBE1	M16	I/P	HPI byte enable 1
HCNTL0	N15	I/P	**Host control register select**
HCS	C16	I/P	**Host chip select**
HD[0]	B16	I/O	**Host data bus 0**
HD[1]	B13	I/O	**Host data bus 1**
HD[2]	B11	I/O	**Host data bus 2**
HD[3]	B15	I/O	**Host data bus 3**
HD[4]	C9	I/O	**Host data bus 4**
HD[5]	C10	I/O	**Host data bus 5**
HD[6]	C11	I/O	**Host data bus 6**
HD[7]	C12	I/O	**Host data bus 7**
HD[8]	C13	I/O	**Host data bus 8**

Table 8.11 TMS320VC5510 Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
HD[9]	C14	I/O	**Host data bus 9**
HD[10]	A15	I/O	**Host data bus 10**
HD[11]	D13	I/O	**Host data bus 11**
HD[12]	D12	I/O	**Host data bus 12**
HD[13]	D11	I/O	**Host data bus 13**
HD[14]	D10	I/O	**Host data bus 14**
HD[15]	D9	I/O	**Host data bus 15**
HDS1	B17	I/P	**Host data strobe 1**
HDS2	D14	I/P	**Host data strobe 2**
HINT	N14	O/P	**Host interrupt (from DSP to host)**
HMODE	N16	I/P	**Host multiplexed/non-multiplexed mode select**
HOLD	U16	I/P	Hold request
HOLDA	P14	O/P	Hold acknowledge
HR/W	C15	I/P	**Host read or write select**
HRDY	B14	O/P	**Host ready (from DSP to host)**
INT0	R12	I/P	**Maskable external interrupt 0**
INT1	U13	I/P	Maskable external interrupt 1
INT2	R13	I/P	Maskable external interrupt 2
INT3	T14	I/P	Maskable external interrupt 3
INT4	P12	I/P	Maskable external interrupt 4
INT5	R11	I/P	Maskable external interrupt 5
IO0	K4	I/P	General-purpose configurable input/output 0
IO1/BOOTM0	M4	I/O	**Boot Mode Selection signal 0**
IO2/BOOTM1	T2	I/O	**Boot Mode Selection signal 1**
IO3/BOOTM2	P1	I/O	**Boot Mode Selection signal 2**
IO4	N2	I/O	General-purpose configurable input/output 1
IO5	M1	I/O	General-purpose configurable input/output 2
IO6	L2	I/O	General-purpose configurable input/output 3
IO7	K1	I/O	General-purpose configurable input/output 4
NM1	T12	I/P	Nonmaskable external interrupt
RST	G16	I/P	**Device reset**
RST_MODE	E17	I/P	Device reset mode control
SDCAS	A13	O/P	SDRAM address column strobe

Table 8.11 TMS320VC5510 Port Assignments (Continued)

Pin Name	Pin No.	Type	Function
SDRAS	A11	O/P	SDRAM row address strobe
SDWE	B12	0/P	SDRAM write enable
SSADS	N4	O/P	SBSRAM address strobe
SSOE	M3	O/P	SBSRAM output enable
SSWE	M2	O/P	SBSRAM write enable
TCK	L17	I/P	**IEEE Standard 1149.1 test clock**
TDI	L16	I/P	**IEEE Standard 1149.1 test data input**
TDO	L16	O/P	**IEEE Standard 1149.1 test data output**
TIN/TOUT0	P15	I/O	Timer 0 input/output
TIN/TOUT1	R17	I/O	Timer 1 input/output
TMS	K14	I/P	**IEEE Standard 1149.1 test mode select**
TRST	C17	I/P	**IEEE Standard 1149.1 test reset**
VSS		PWR	Ground
XF	B2	O/P	External flag output

8.5 Appendix E – Component Locations

This table indicates where components may be found on the PCB layout (by grid reference) or on the schematics (by sheet number and grid reference). For clarity, IC power connections and power supply bypass capacitors have been omitted from this table.

This table is applicable to version 2A (220-2056-02) only.

Table 8.12 Component Locations

Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref
C100	N8	1F2	C604	D2	6H3	C913	P7	9E7
C101	N7	1E3	C605	C2	6G3	C914	M7	9F7
C102	M8	1H3	C606	E2	6F3	C915	L5	9G7
C103	M8	1F3	C607	D2	6F3	C916	N7	9E7
C104	H7	1B3	C608	D2	6E3	C917	M6	9H7
C105	M8	1H3	C609	K5	6D3	C918	L7	9F9
C106	N8	1E3	C615	N4	6E7	C919	H5	9D10
C107	N8	1F3	C619	N4	6B3	C920	N6	9H5
C108	M8	1H3	C629	K5	6C4	C921	K6	9H9
C109	H7	1B3	C639	J5	6J7	C922	K7	9G9
C210	D3	2F11	C649	M4	6G7	C923	J7	9H13
C317	C7	3D3	C650	M4	6F7	C925	N7	9E4
C500	N3	5E2	C651	J5	6F7	C926	N7	9E7
C504	P3	5D4	C652	M4	6E7	C929	M7	9F11
C505	P3	5D5	C653	L5	6D7	C930	J7	9H10
C506	P3	5C5	C654	J5	6C7	C939	H6	9D11
C507	N1	5F10	C655	J4	6K7	C949	G5	9D12
C508	N2	5D10	C656	J4	6K8	C959	J7	9H12
C509	L2	5F10	C657	P5	6C8	C969	G6	9D13
C510	L3	5D10	C658	J4	6J8	C970	J7	9H13
C511	K1	5F11	C723	E2	7F12	C972	K6	9F13
C512	K2	5D11	C804	G6	8E4	C973	H6	9D13
C513	H2	5J11	C805	G5	8E5	D101	K7	1H3 1F3
C514	H2	5H11	C900	J6	9G2	D201	D3	2G10 2F11
C515	L2	5F11	C901	L7	9J2	D500	L3	5H10 5H9

Table 8.12 Component Locations (Continued)

Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref
C516	K3	5D11	C902	N7	9G2	D501	H3	5J11
C517	N2	5F6	C903	L6	9J3	D502	H3	5H11
C518	N4	5E6	C904	P7	9G3	D503	K1	5F11
C519	N2	5D6	C905	M5	9H4	D504	K2	5D11
C520	N1	5E7	C906	N5	9H4	D505	N2	5C9
C521	M1	5F9	C907	M6	9H5	D506	N1	5F9
C522	N2	5E9	C908	N7	9E5	D507	N1	5E10
C600	D2	6J2	C909	M5	9G5	D600	K5	6E6 6D6
C601	D2	6C2	C910	N7	9F5	D601	P5	6B4
C602	C2	6B2	C911	P7	9E5	D602	J4	6C4
C603	D2	6J3	C912	N6	9H6	D603	H4	6H5
D604	J6	6J5	E507	J1	5D12	Q901	M5	9F8 9G8
D605	M4	6E6	E508	J2	5C12	Q902	K7	9H9
D606	P4	6H13	E600	D2	6J3	Q903	K7	9G9
D610	L5	6H12	E601	D2	6H3	Q910	L7	9B12
D700	G3	7F9	E602	C2	6G3	R100	K6	1E2
D900	M5	9G5 9G7	E603	E2	6G3	R101	N8	1H4
D901	H7	9F12	E604	D2	6F3	R102	G7	1C13
D902	H7	9E12 9F12	E605	D2	6E3	R110	L8	1H4
D903	J8	9C12	E606	K5	6D3	R111	M8	2E2 2G2 2D2
D904	P6	9G4	E607	D2	6D3	R112	N7	1G4
D905	M6	9F8	E608	C2	6B3	R113	N7	1G4
D906	K5	9E12	E700	H5	7H4	R200	B6	2A2
D907	G7	9E12	E900	L7	9J3	R201	C3	2C5
D908	K7	9G8	E901	P7	9G2	R202	A4	2D10 2D9 2G7
D909	K6	9H10 9G10	E902	M7	9G10	R203	C3	2C5
D910	K7	9H9 9G9	E910	H6	9D12	R204	D4	2C5
D911	J7	9H9	F501	H2	5K12	R205	B6	2C6
DS100	G1	1F12	F503	H2	5J12	R206	A6	2G7
DS101	E1	1F12	F505	K2	5F12	R207	A3	2F7
DS200	B1	2H2	F507	L3	5D12	R208	B3	2F7 2E7

Table 8.12 Component Locations (Continued)

Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref
DS400	A1	4G8	F600	K4	6D3	R209	D4	2J7
DS500	M3	5J8	F601	H4	6J4	R210	C3	2E7
E100	H7	1C3	F900	L7	9J2	R211	A5	2G7 2F7
E101	H7	1C3	J100	B2	1J2	R212	A5	2F7 2G7
E102	G7	1C3	J101	M8	1G2	R213	F5	7F7
E103	H7	1B3	J102	H8	1C2	R213	F5	6C6
E104	H7	1C3	J103	D2	1J13	R213	F5	5J6
E105	H7	1B3	J104	F2	1G13	R213	F5	2D1 2E5
E106	G7	1B4	J105	H2	1D13	R214	B1	2E5
E107	M7	1G5	J108	L5	1H13	R215	B1	2D5
E108	M7	1G5	L200	C2	2B11	R216	J5	2C5
E109	M7	1H5	L900	P6	9G3	R217	B1	2H2
E110	M7	1G5	L901	M6	9G9	R218	B3	2A2
E111	N7	1G5	L910	H5	9D11	R219	B3	2F7
E112	N7	1F5	Q500	L3	5H10	R220	A4	2F7 2C10 2C9
E500	N3	5F2	Q501	K6	6C6	R221	A5	2F7 2G7 2C10 2D10
E501	H2	5K12	Q501	K6	5J7	R222	C6	2H2
E502	H2	5J12	Q503	K3	5H9	R223	D3	2G11
E503	H2	5J12	Q504	K4	5G10 5H9	R224	D3	2F11
E504	H2	5G12	Q600	K5	6C5	R225	P3	6H12
E505	J1	5F12	Q603	N4	6A9 6A8	R300	C7	3D4
E506	J1	5E12	Q900	P5	9G4	R301	A6	3F5
R302	A6	3F5	R632	L5	6H4	R903	N7	9F4
R303	C7	3D3	R633	L5	6H4	R904	M7	9E5
R400	F6	4E3	R634	K5	6H5	R905	N5	9H6
R401	F5	4E4	R636	K5	6H5	R906	M7	9E7
R402	F4	4G7 4F5 4G8	R637	M4	6G5	R907	K8	9D8
R403	F5	4G8	R638	M4	6G5	R908	M7	9G9
R404	G8	4E3	R639	N4	6F5	R909	M7	9F9
R405	H7	4E3	R640	N4	6E5	R910	M7	9E9

Table 8.12 Component Locations (Continued)

Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref
R406	A1	4G8	R641	L5	6D5	R911	K7	9C8
R407	F6	4E7	R643	K6	6C6	R912	P7	9F5
R408	H7	4B3	R650	J5	6D7	R913	P7	9F7
R500	N2	5E2	R651	N4	6B7	R920	H6	9D11
R501	P3	5C4	R657	N4	6B8	R921	H6	9D11
R502	P2	5F6	R658	N4	6B8	R922	J5	2F5 6C6 9C12 9B12
R503	N3	5K7	R660	P5	6C9	S900	K8	9C8
R504	N2	5D5	R661	N5	6C9	T500	M1	5F10
R505	N2	5D5	R662	N5	6A9	T501	M2	5D10
R506	N3	5K8	R663	N5	6B10	T700	G3	7G11
R507	L4	5H9	R700	G5	7F2	TP200	A5	2H1
R508	N2	5D9	R701	F4	7E2	TP201	A7	2H1
R509	N2	5C9	R703	G4	7E6	TP202	A5	2D1
R510	P4	5F5	R705	F3	7F9	TP203	A3	2D1
R511	N4	5E5	R706	F3	7F10	TP204	A4	2C1
R512	L4	5H9	R708	F4	7D7	TP205	A6	2C1
R513	L4	5H9	R708	F4	4C8	TP206	A7	2H1
R514	L3	5G9	R710	G3	7F10	TP207	A3	2D1
R515	L4	5G10	R711	G3	7F10	TP208	A6	2D1
R516	P2	5E7	R712	F3	7F12	TP209	A3	2D1
R517	P2	5D6	R713	F3	7F12	TP210	A4	2B10
R520	P2	5F7	R714	E1	7E13	TP211	A4	2B10
R521	N1	5F7	R715	G1	7E13	TP212	A5	2B10
R522	N2	5E7	R716	F2	7F13	TP213	C7	2B10
R530	N1	5F8	R717	F2	7F13	TP214	A4	2B10
R531	N2	5E8	R801	F3	8D3	TP215	A6	2B11
R532	N1	5F8	R802	G6	8E4	TP216	A5	2B11
R533	N1	5E8	R803	G6	8E4	TP217	A6	2B11
R534	N2	5E8	R804	E4	8E6	TP218	A7	2B11
R535	N2	5F8	R805	E4	8D6	TP219	A7	2B11
R600	K5	6D3	R806	E4	8D6	TP220	A2	2B10

Table 8.12 Component Locations (Continued)

Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref	Cpt Ref	PCB Grid Ref	Schematic Sheet / Grid Ref
R601	P4	6B3	R807	G6	8E5	TP221	A2	2E9
R602	K5	6D5	R808	G5	8E6	TP222	A2	2C11
R620	H4	6H3	R900	N7	9F3	TP223	A3	2B7
R630	L5	6H4	R901	N7	9F3	TP400	E4	4G7
R631	P4	6B7	R902	N7	9G3	TP401	E4	4G7
TP402	E4	4G7	U202	H5	2B6	U601	N4	5F6
TP403	D4	4F7	U203	E4	2D13 2B5	U602	J5	6E8 6C13 6F8 6D8 6G8
TP404	F4	4G7	U204	D4	2G12 2B13	U700	G4	7F5
TP405	E4	4F7	U205	D5	2B13 2H12	U701	F4	7C6 7C13
TP406	E3	4E8	U210	D4	2J12 2D14	U800	G5	8A6 8E6
TP407	D3	4E8	U211	D4	2D13 2J12	U801	F3	8D6 8A7
TP408	E3	4D8	U212	D3	2G11 2B14	U900	N6	9F6
TP409	E3	4E8	U213	D3	2G11 2D14	U901	K8	9C8
TP410	E3	4D8	U300	B7	3D6	U902	J7	9H12
TP411	F4	4D8	U301	F7	3H9	U910	H5	9D11
TP412	E6	4D8	U302	D7	3D9	W200	D3	2B12
TP413	D3	4H8	U400	E5	4F12 4G6 4A9	W201	E1	2E5
TP900	P8	9A11	U500	N3	5D4	W900	N6	9E6
TP910	A2	9A11	U501	P2	5E8 5A7 5F8	Y200	G5	8E5
U200	E4	2B12 2J12	U600	J4	6J8			
U201	B4	2A9 2E4 2G8	U601	N4	6G13 6B8			